1.1 Basics of operational amplifier:

An integrated circuit is a collection of discrete elements (diodes, resistors, capacitors & transistors) created by means of a single construction process in which all the elements are formed.

→ An Integrated circuit consists of a single crystal chip of silicon, containing both active and passive elements and their interconnections.

→ IC is a miniature, low cost electronic circuit consisting of active and passive components together on the same silicon chip.

→ Large and complex circuits can be reduced to a small size by IC technology.

→ The IC complexity has advanced from small - scale integration (SSI) to medium scale integration (MSI), to large scale integration and finally to very large scale integration (VLSI).

The main components used to manufacture ICs are diode, transistors, resistor and capacitors.

Transistors are either bipolar or unipolar type. Bipolar transistors are of two types, npn and pnp. Unipolar transistors are mainly MOSFETs. There are two types of MOSFETs,

1) n-channel MOSFETs
2) p-channel MOSFETs.

Further it is classified as
1) enhancement mode and
2) depletion mode.

1.1.1 Classification of Integrated circuits

The categories of IC's based on fabrication are

1) Monolithic
2) Hybrid ICs.

The categories of IC's based on application are

1) Analog ICs
2) Digital ICs.

Monolithic ICs:

All circuit components both active and passive elements and their interconnections are manufactured into or on top of a single chip of silicon.

Hybrid ICs:

In hybrid circuits, seperate component parts are attached to a ceramic substrate and interconnected by means of metallisation pattern.

Analog IC:

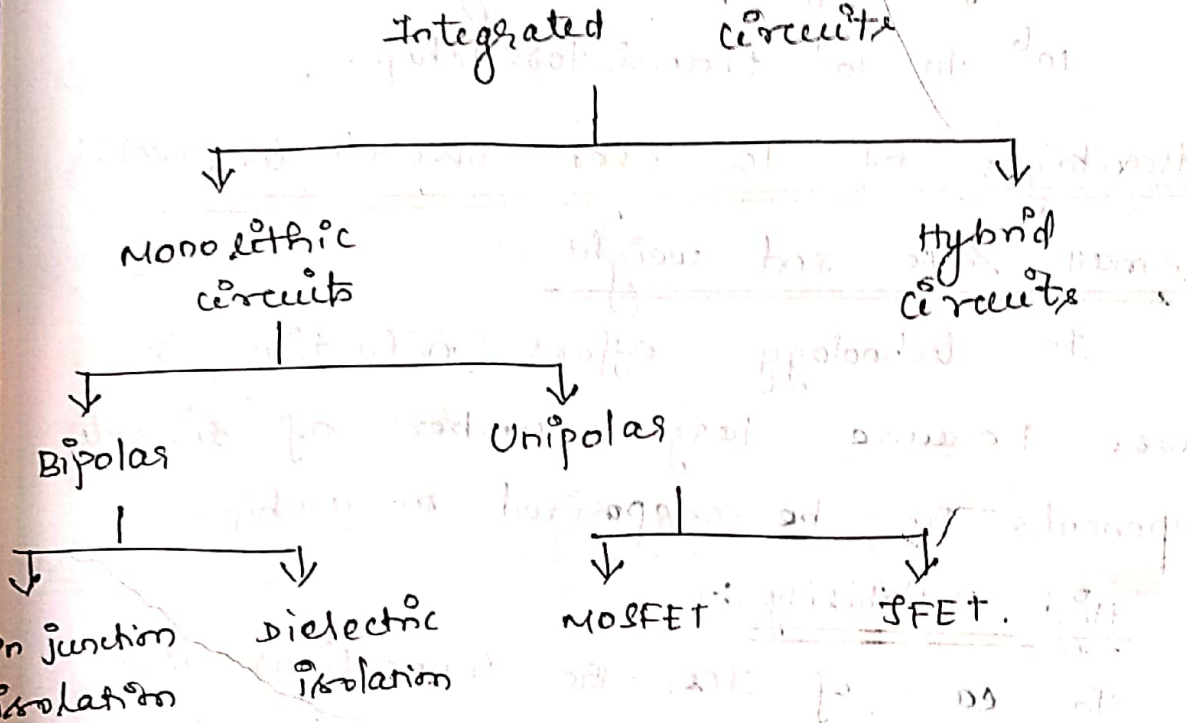
An analog IC is one which performs amplification or essentially linear operation on signals. It is also known as linear IC.

It deals with continuously varying quantities such as temperature, pressure,

Digital IC :-

Digital IC performs the circuits functions dealing with discrete quantities (ie) integer or factional number.

Digital Ic involve logic gates and memory, for application in computers, calculators microprocessors.



1.2 Levels of Integrated circuit (IC) :

The different levels of Integration of IC chips are

1) SSI (Single scale Integration)

The no of logic gates on a chip is lower than 10.

2) MSI (Medium scale Integration)

The no of logic gate on a chip is between 10 to 100.

LSIC (large scale Integration)

The no. of logic gates on a chip is between 100 to 10,000.

VLSI (very large scale Integration)

The no of logic gates on a chip is more than 10,000.

VLSIC (Ultra very large scale Integration).

10^6 to 10^7 transistors/chip.

1.1.3 Advantages of ICs over Discrete Components:

1) Small size and weight :-

IC technology offers reduction in size. Because large number of discrete components can be deposited on a chip.

2) High Reliability :

In case of ICs, the connections are part of a package, there are few external connections to solder and the reliability is high. (All components are fabricated simultaneously and there are no soldered joints.

3) Low cost :

Since hundreds of external circuits can be built simultaneously on a single silicon wafer the circuit cost is reduced.

4. Reduction in power consumption :-

Logic gates inside chips have lower noise disturbances, allowing the use of lower signal voltage levels consequently reducing power consumption.

5. Improvement in speed :-

With ICs, the various applications can work with great speed.

6. Improved functional performance :-

Because of the low cost, more complex circuitry may be used to obtain better functional characteristics.

1.6 Basic information about op-amps :-

The operational amplifier was introduced in 1947 by John R. Ragazini to denote that a special type of amplifier, could be configured for a variety of operations such as amplification addition, subtraction, differentiation and Integra

1.6.1 Features :-

1. It is a multiterminal devie
2. It is internally quite complex.
3. It has two input terminals and one output terminal.
4. The terminal (-) → Inverting terminal.
   The terminal (+) → non inverting terminal.
5. In three packages, this op-amp is availab
   a) Metal can package
   b) The dual in line package
   c) The flat package.
6. The opamp packages may have single, two (dual), or four (quad) opamps.

7. Typical packages have either 8 or 10 or 14 terminals.

8. The widely used very popular type is µA741. It is a single opamp and is available as an 8 pin can, 8 pin DIP or 10 pin flatpack or 14 pin DIP.

1.6.2 Circuit symbol :-

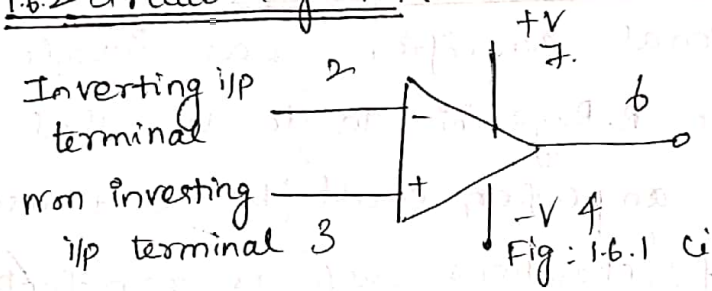


Fig : 1.6.1 Circuit symbol.

There are five basic terminals

1) Two input terminals
2) One output terminal
3) Two power supply terminals (±V)

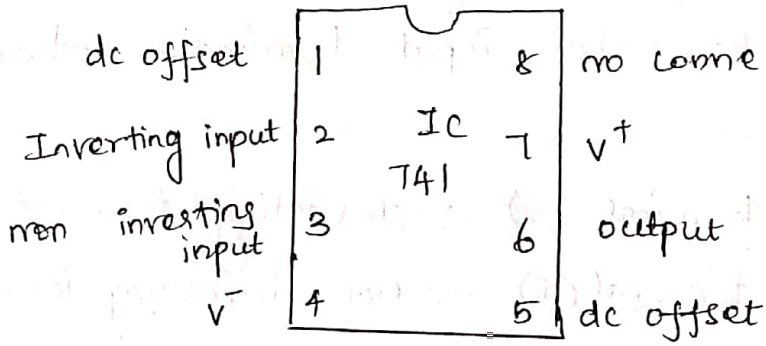


Fig : 1.6.2 Pin diagram.

1.6.3 Power supply connections :-

The V^+ and V^- power supply terminals are connected to two dc voltage sources.

The V^+ pin is connected to the positive terminal of one source and the V^- pin is connected to the negative terminal

of the other source. The common terminal of the V^+ and V^- sources is connected to a reference point or ground. Some op amps have a ground terminal. but most do not.

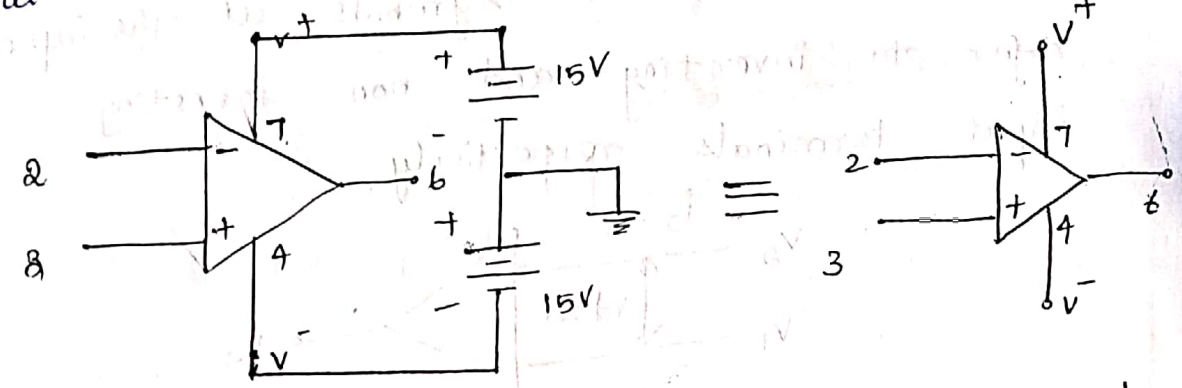
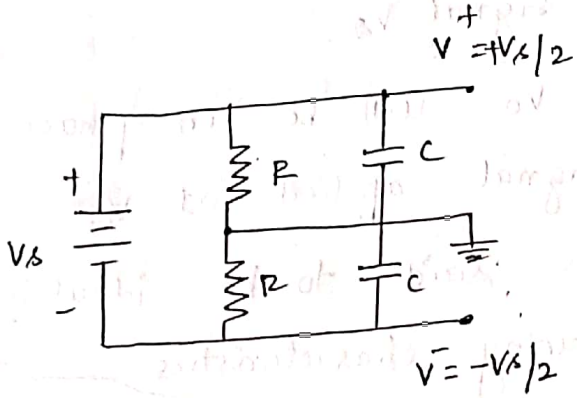


Fig: 1.6.3 Power supply connections

Fig: 1.6.4 Circuit symbol showing power supply terminals.



The resistor R should be greater than 10 KΩ so that it does not draw more current from the supply Vs.

The capacitors provide decoupling the power supply and range in value from 0.01 to 10 μF.

1.6.4 Ideal operational amplifier:-

The schematic symbol of an op-amp has two input terminals one output terminal. other terminals have not been shown for simplicity.

The - and + symbols at the input refer to inverting and non inverting input terminals respectively.

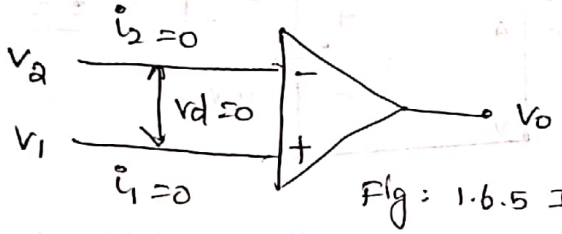


Fig: 1.6.5 Ideal op amp.

If $V_1 = 0$, output V_o is 180° out of phase with input signal V_2.

when $V_2 = 0$, output V_o will be in phase with the input signal applied at V_1.

This op-amp is said to be ideal if it has the following characteristics.

1) Infinite voltage gain
2) Infinite Input impedance
3) zero output impedance
4) zero offset voltage
5) Infinite bandwidth
6) Infinite CMRR
7) Infinite slew rate
8) No effect of temperature 9) zero PSRR.

These ideal characteristics of opamp are summarized

D. Roychoudhury Shail. B. Jain "Linear Integrated"

Open loop voltage gain	A_{OL}	$= \infty$
Input impedance	R_{in}	$= \infty$
output impedance	R_o	$= 0$
offset voltage	V_{oo}	$= 0$
Bandwidth	BW	$= \infty$
CMRR	ρ	$= \infty$
Slew rate	δ	$= \infty$
Power supply rejection ratio	PSRR	$= 0$

1.6.5 Ideal voltage Transfer curve:

The Ideal op amp produces the output proportional to the difference between the two input voltages. The graphical representation of this statement gives the voltage transfer curve.

It is the graph of output voltage V_o plotted against the difference input voltage V_d assuming gain constant. This graph is called transfer characteristics of the op amp.

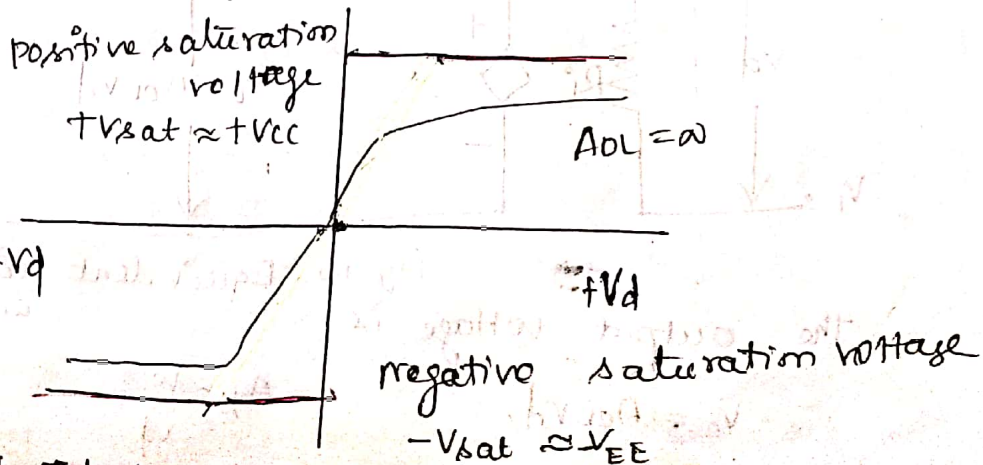


Fig: 1.6.6 Ideal voltage transfer curve

From the ideal characteristics of differential amplifier, it can be seen that

1) An ideal op-amp draws no current at both the input terminals. (ie) $I_1 = I_2 = 0$, because of Infinite input impedance, any signal source can drive it and there is no loading on the preceeding driver stage.

2) since gain is ∞, the voltage between the inverting and non inverting terminals (ie) differential output voltage $V_d = V_1 - V_2$ is essentially zero for finite output voltage V_o.

$$A_d = \frac{V_o}{V_d} = \frac{\text{finite o/p voltage}}{0} = \infty.$$

A physical amplifier is not an ideal one. so the equivalent circuit of the op-amp is shown in figure. where $A_{OL} \neq \infty$, $R_i \neq \infty$, $R_o \neq 0$.

Equivalent circuit of an op-amp

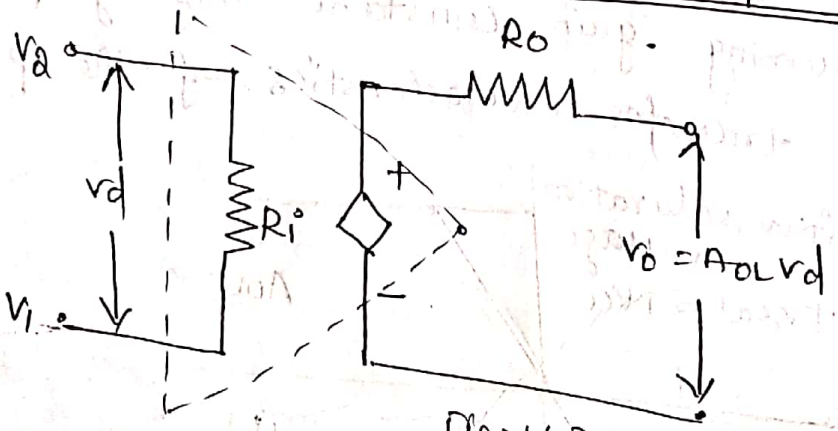


Fig: 1.6.7 Equivalent Circuit of an opamp

The output voltage is

$V_o = A_{OL} V_d$.

$$A_{OL} = \frac{V_o}{V_d}$$

$$V_o = A_{OL}(V_1 - V_2)$$

The equation shows that the op-amp amplifies the difference between the two input voltages.

1.6.6 General operational amplifier stages :-

Commercial integrated circuit op-amps usually consists of four cascaded blocks. The first two stages are cascaded differential amplifiers and are designed to provide high gain and high input resistance.

The third stage acts as a buffer as well as a level shifter.

The final stage is output stage. It is designed to provide low output impedance.

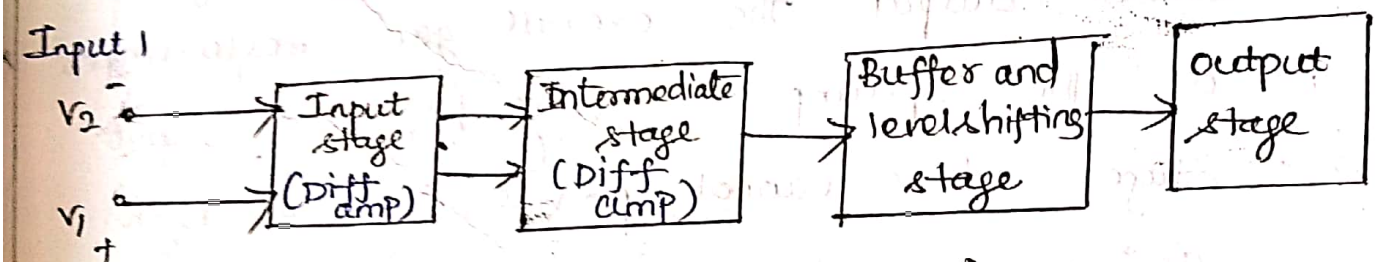


Fig: 1.6.8 Internal block schematic of op-amp.

1) Input stage :

The Input stage provides high input impedance to prevent loading on the high gain stage.

It requires two input terminals.

It also requires low output impedance. All such requirements are achieved by using dual input, balanced output differen amplifier as the input stage.

The function of the differential amplifier is to amplify the difference between the two input signal.

The differential amplifier has high input impedance. This stage provides most of the voltage gain of the amplifier.

2) Intermediate stage:

The output of the input stage drives the next stage which is an intermediate stage.

This is another differential amplifier with dual input, unbalanced (ie) single ended output. The overall gain requirement of the op-amp is very high. The input stage alone cannot provide such a high gain.

The main function of the intermediate stage is to provide an additional voltage gain required.

Practically, the intermediate stage is not

a single amplifier, but the chain of cascaded amplifiers called multistage amplifiers.

3) Buffer and level shifting stage :-

The op-amp amplifies d.c signals also, the coupling capacitors are not used to cascade the stages. capacitor → blocks dc and allows ac signal

Hence the d.c quiescent voltage level of previous stage gets applied as the input to the next stage.

Hence stage by stage d.c level increases well above ground potential. such a high d.c voltage level may drive the transistors into saturation.

This further may cause distortion in the output due to clipping.

Hence before the output stage, it is necessary to bring such a high d.c voltage level to zero volts with respect to ground.

The level shifter stage brings the d.c level down to ground potential, when no signal is applied at the input terminals.

Then the signal is given to the last stage which is the output stage.

The buffer is usually an emitter follower whose input impedance is very high.

4) Output stage :

The output stage is designed to provide low output impedance, large a.c output voltage swing & high current sourcing and sinking capability.

The push pull complementary amplifier meets all these requirements and hence used as an output stage.

The stage raises the current supplying capability of the op-amp.

Intermediate stage :

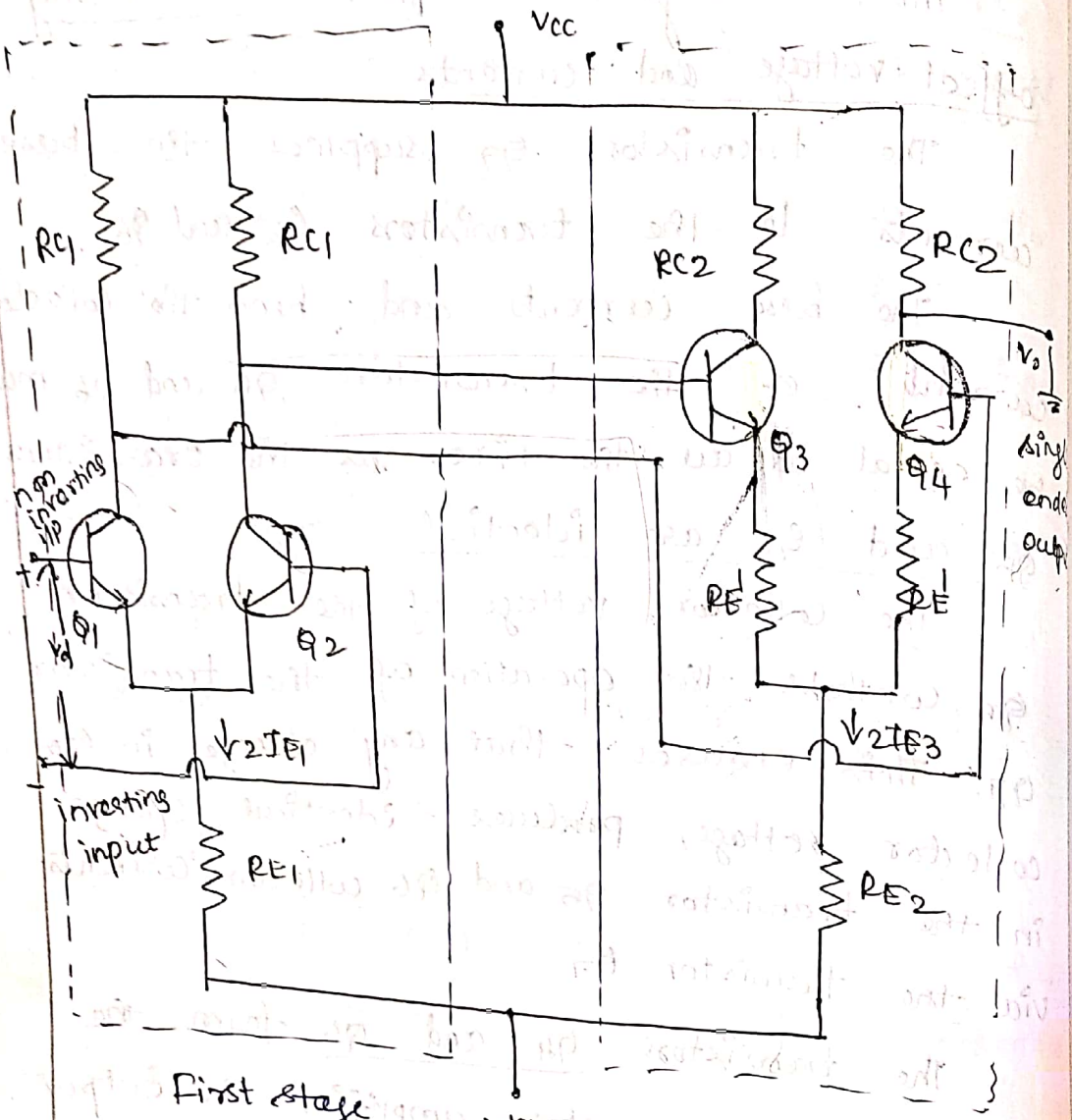


fig:17. Input and intermediate stage in an op-amp with dual input, unbalanced (ie) single ended output.

The overall gain requirement of the op-amp is very high. The input stage alone cannot provide such a high gain.

The main function of the intermediate stage is to provide additional voltage gain

Simple level shifting network

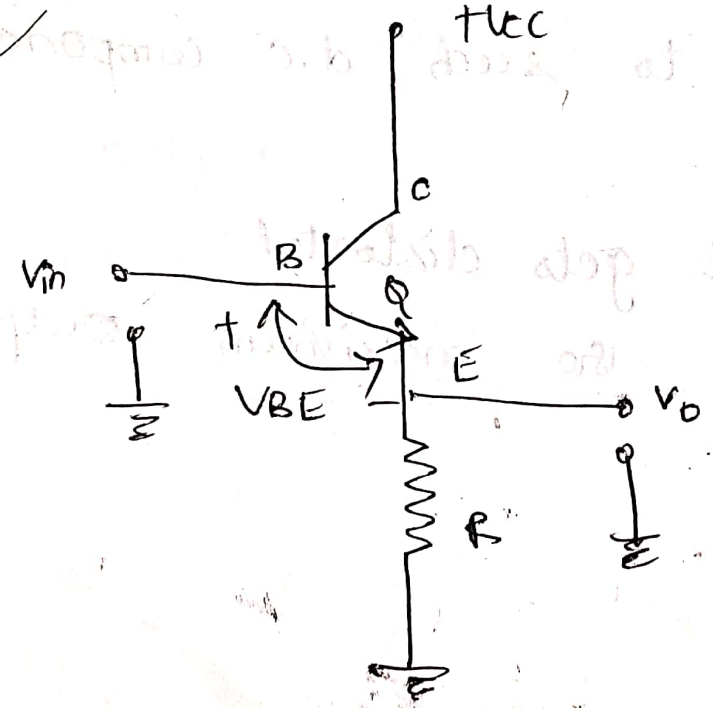


Fig 1.6.5 Simple level shifting network

1.7.4 Output stage :-

The output stage of op-amp supplies the load and provides low output impedance. The requirements of good output stage are

1) Large output voltage swing capability
2) Large output current swing capability
3) Low output impedance
4) Low quiescent power dissipation.
5) Short circuit protection.

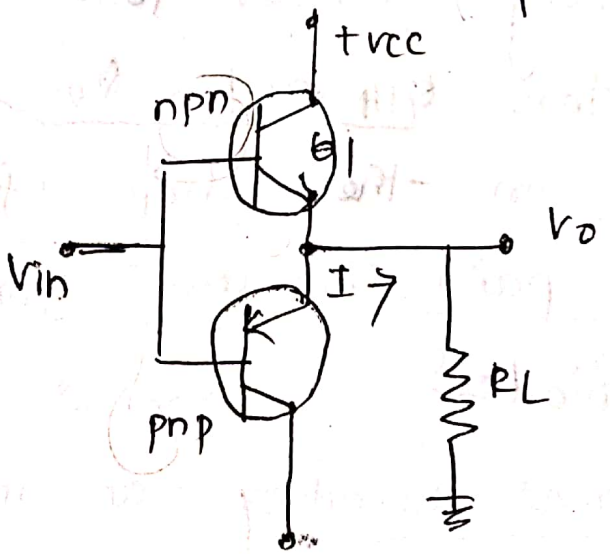


Fig: 1.6 Output stage of an op-amp

1.13 Open and Closed loop configurations :

1.13.1 Open loop configuration of op-amp :-

The term open-loop indicates that no feedback in any form is fed to the input from the output. When connected in open-loop the op-amp function as a very high gain amplifier.

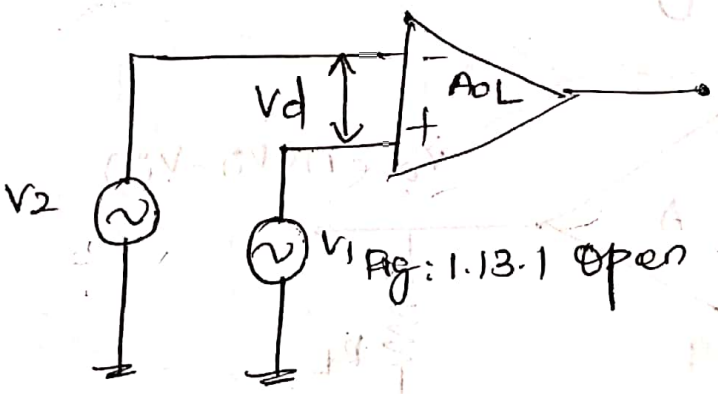


Fig: 1.13.1 Open loop operation of op-amp

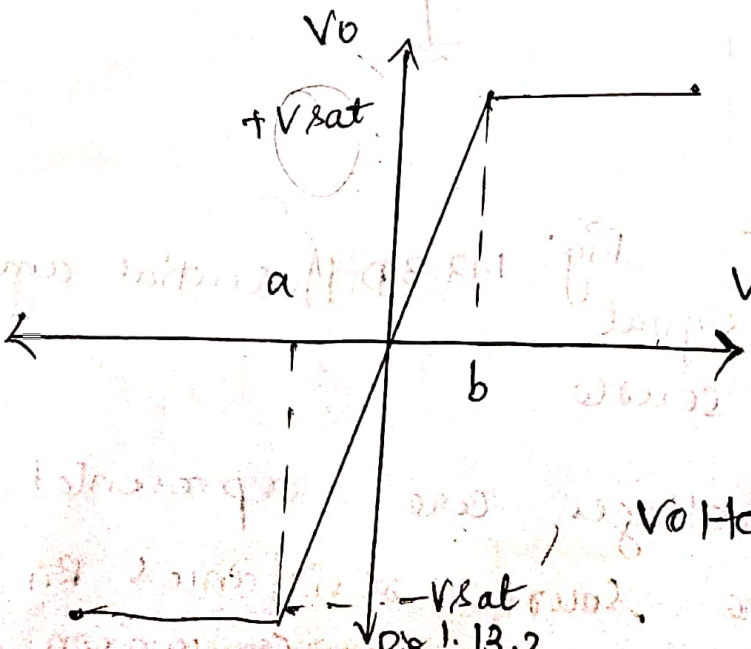


Fig 1.13.2 Voltage transfer characteristics

There are three open loop configurations of op-amp,

1) Differential amplifies
2) Inverting amplifies
3) non-Inverting amplifies

1.13.1.1) Open loop differential amplifies :

In this configuration, the inputs are applied to both the inverting and the non-inverting input terminals of the op-amp and it amplifies the difference between the two input voltages.

Figure shows the open-loop differential amplifies configuration.

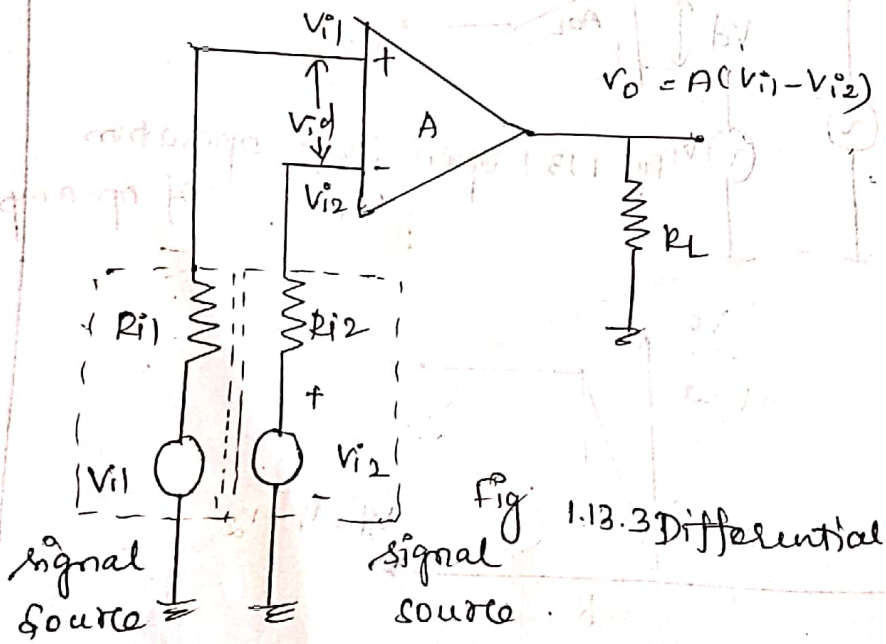


Fig 1.13.3 Differential amplifies

The input voltages are represented by V_{i1} and V_{i2}. The source resistances R_{i1} and R_{i2} are negligibly small in comparison with

with the very high input resistance offered by the op-amp.

$$V_o = A(V_{i1} - V_{i2})$$

where A is the large signal voltage gain. Thus the output voltage is equal to the voltage gain A times the difference between the two input voltages.

1.13.1.2) Inverting amplifier :

In this configuration, the input signal is applied to the inverting input terminal of the op-amp and the non-inverting input terminal is connected to the ground.

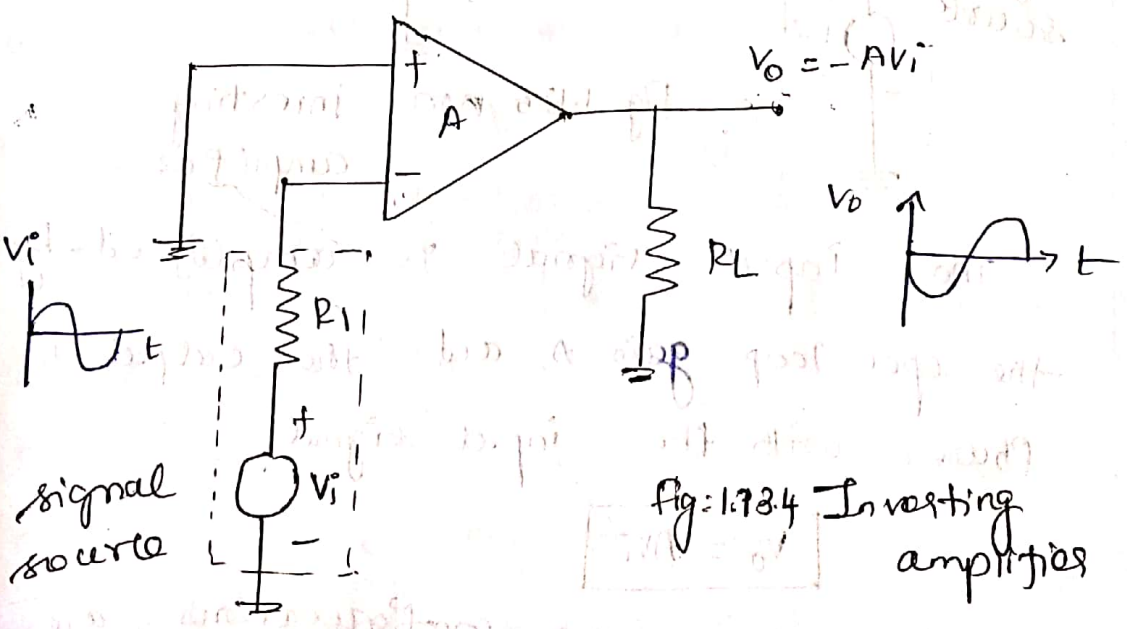


fig: 1.13.4 Inverting amplifier

The output voltage is 180° out of phase with respect to the input and hence the output voltage V_o is given by

$$V_o = -AV_i$$

Thus in an inverting amplifier, the input signal is amplified by the open-loop gain A and is phase-shifted by 180°.

1.13.13) Non-inverting amplifier :-

The input signal is applied to the non-inverting input terminal of the op-amp and the inverting input terminal is connected to the ground.

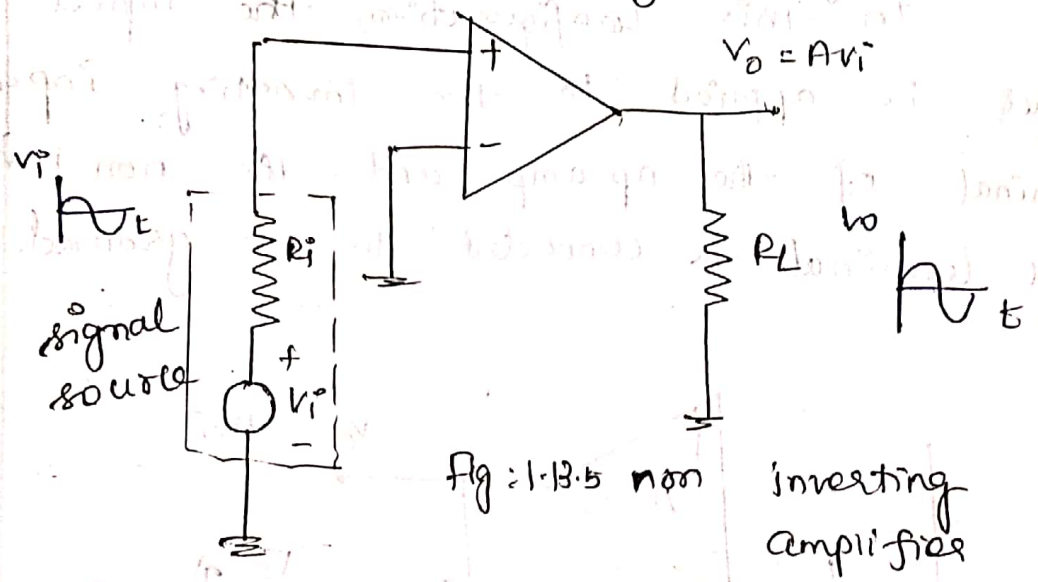


fig : 1.13.5 non inverting amplifier

The input signal is amplified by the open loop gain A and the output is in phase with the input signal.

$$V_o = AV_i$$

These open loop configurations are rarely used in op-amp practice.

1.13.2 Closed loop configuration of op-amp :-

The utility of op-amp increases considerably if it is used in a closed loop mode. The closed loop mode is possible using feedback.

The feedback allows to feed some part of the output back to the input.

The negative feedback is possible by adding a resistor called feedback resistor. The feedback is said to be negative as the feedback resistor connects the output to the inverting input terminal. The gain resulting with feedback is called closed loop gain of the op-amp. Due to feedback resistance there is reduction in the gain.

2.3 Inverting amplifier :-

As the name suggests the output of such an amplifier is inverted as compared to the input signal. The inverted output signal means having a phase shift of 180° as compared to the input signal.

So, an amplifier which provides a phase shift of 180° between input and output is called inverting amplifier.

The basic circuit diagram of an inverting amplifier is shown in figure.

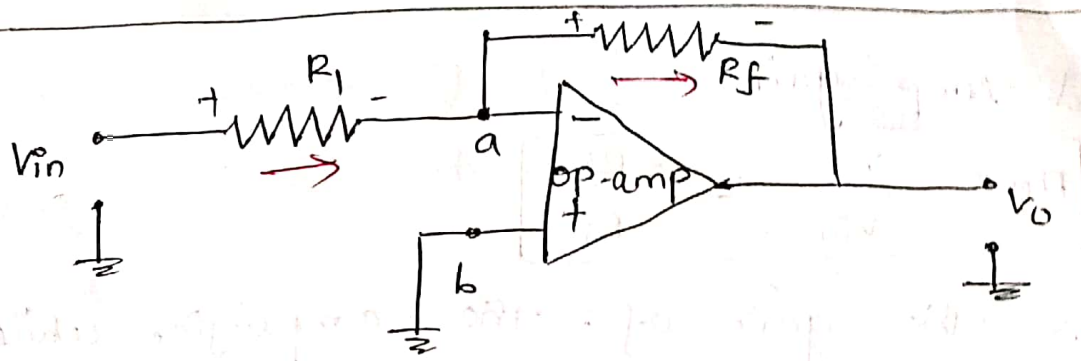


Fig 2.3.1 Inverting amplifier.

As node b is grounded, node a is also at ground potential, from the concept of virtual ground, so $V_a = 0$

$$I = \frac{V_{in} - V_a}{R_1}$$

$$I = \frac{V_{in}}{R_1} \quad \text{——} (1)$$

From the output side, considering the direction of current I we can write

$$I = \frac{V_a - V_o}{R_f}$$

$$I = \frac{-V_o}{R_f} \quad \text{——} (2)$$

Entire current I passes through Rf as op-amp input current is zero.

equating (1) and (2)

$$\frac{V_{in}}{R_1} = \frac{-V_o}{R_f}$$

Closed loop gain

$$A_{CL} = \frac{V_o}{V_{in}} = \frac{-R_f}{R_1}$$

$\frac{R_f}{R_1}$ is the gain of the amplifier while negative sign indicates that the polarity of the output is opposite to that of input. Hence it is called inverting amplifier.

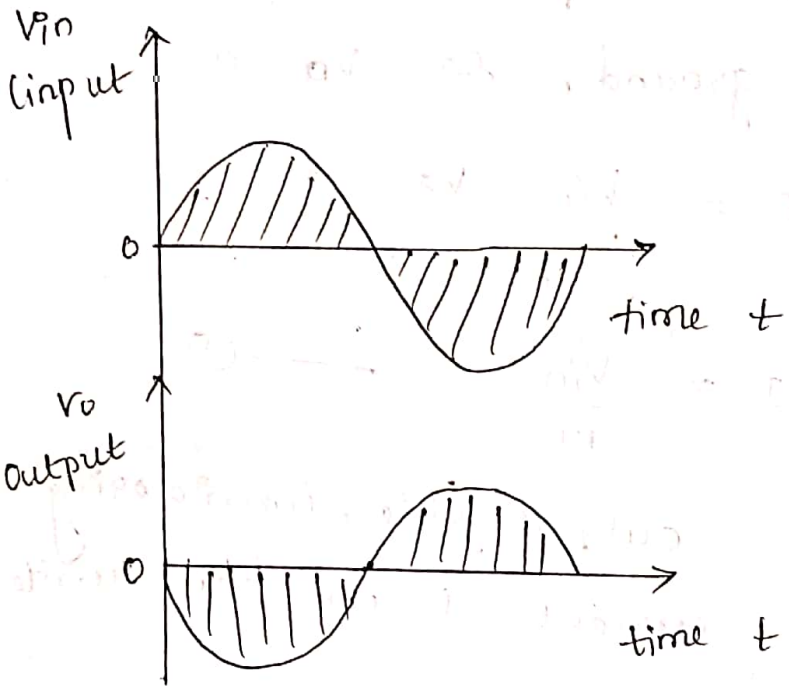


Fig 2.3.2 waveforms of inverting amplifier

If $R_f > R_1$ the gain is greater than 1

if $R_f < R_1$ the gain is less than 1

if $R_f = R_1$, the gain is unity.

Thus the output voltage can be greater than, less than or equal to the input voltage in magnitude.

If the ratio of R_f and R_1 is k which is other than one, the circuit is called scale changes.

while for $R_f/R_1 = 1$ It is called sign changes or phase shifter.

2.3.1 sign changer :-

In the inresting amplifier if $R_f = R_1$ then the gain $A_{CL} = -1$. Thus the magnitude of the output is same as that of the input but its sign is opposite to that of the input.

$$A_{CL} = \frac{V_o}{V_{in}} = \frac{-R_f}{R_1}$$

if $R_f = R_1$

$$A_{CL} = \frac{V_o}{V_{in}} = -1$$

$$\Rightarrow \boxed{V_o = -V_{in}}$$

This circuit is called sign changes or phase Inverter.

2.3.2 Scale changer :-

In the inverting amplifier if $R_f \neq R_1$ then the gain is $A_{CL} = -K$ where $K = \frac{R_f}{R_1}$. Thus the circuit is used to multiply inp by a constant k called scaling factor.

$$V_o = -KV_{in}$$

For an inverting amplifier

$$A_{CL} = \frac{V_o}{V_{in}} = \frac{-R_f}{R_1}$$

Take $\frac{R_f}{R_1} = K$.

$$\therefore \quad \frac{V_o}{V_{in}} = -K$$

$$\boxed{V_o = -KV_{in}}$$

This circuit is called scale changer.

2.4 Non inverting amplifier :-

An amplifier which amplifies the input without producing any phase shift between input and output is called non inverting amplifier. The input is applied to the non inverting input terminal of the Op-amp.

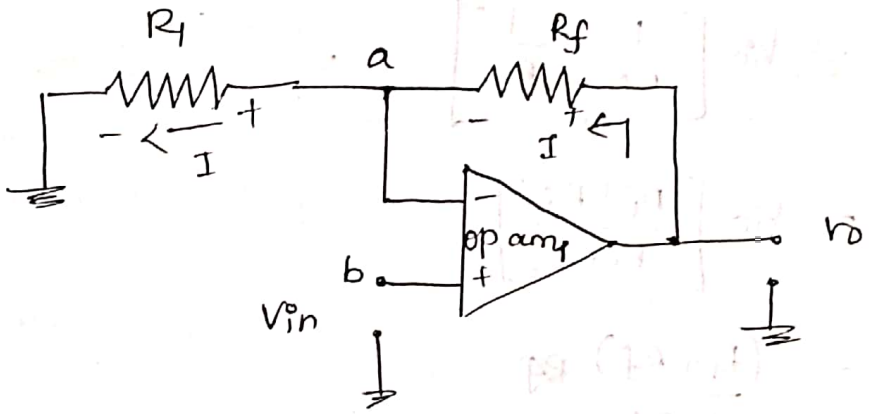


Fig 2.4.1 non inverting amplifier.

The node b is at potential Vin, hence the potential of point A is same as B which is Vin from the concept of virtual ground.

$$V_a = V_b = V_{in}$$

From the output side we can write.

$$I = \frac{V_o - V_a}{R_f}$$

$$= \frac{V_o - V_{in}}{R_f} \quad \text{—(1)}$$

At the inverting terminal.

$$I = \frac{V_a - 0}{R_1} = \frac{V_a}{R_1} = \frac{V_{in}}{R_1} \quad \text{—(2)}$$

From (1) and (2)

$$\frac{V_o - V_{in}}{R_f} = \frac{V_{in}}{R_1} \quad \text{or} \quad \frac{V_o}{R_f} - \frac{V_{in}}{R_f} = \frac{V_{in}}{R_1}$$

$$\frac{V_o}{R_f} = V_{in}\left[\frac{1}{R_f} + \frac{1}{R_1}\right]$$

$$\frac{V_o}{R_f} = V_{in}\left[\frac{R_1 + R_f}{R_1 R_f}\right]$$

$$\frac{V_o}{V_{in}} = \frac{(R_1 + R_f)\,R_f}{R_1 R_f}$$

$$= \frac{R_1 + R_f}{R_1}$$

$$\boxed{A_f = \frac{V_o}{V_{in}} = 1 + \frac{R_f}{R_1}}$$

The positive sign indicates that there is no phase shift between input and output.

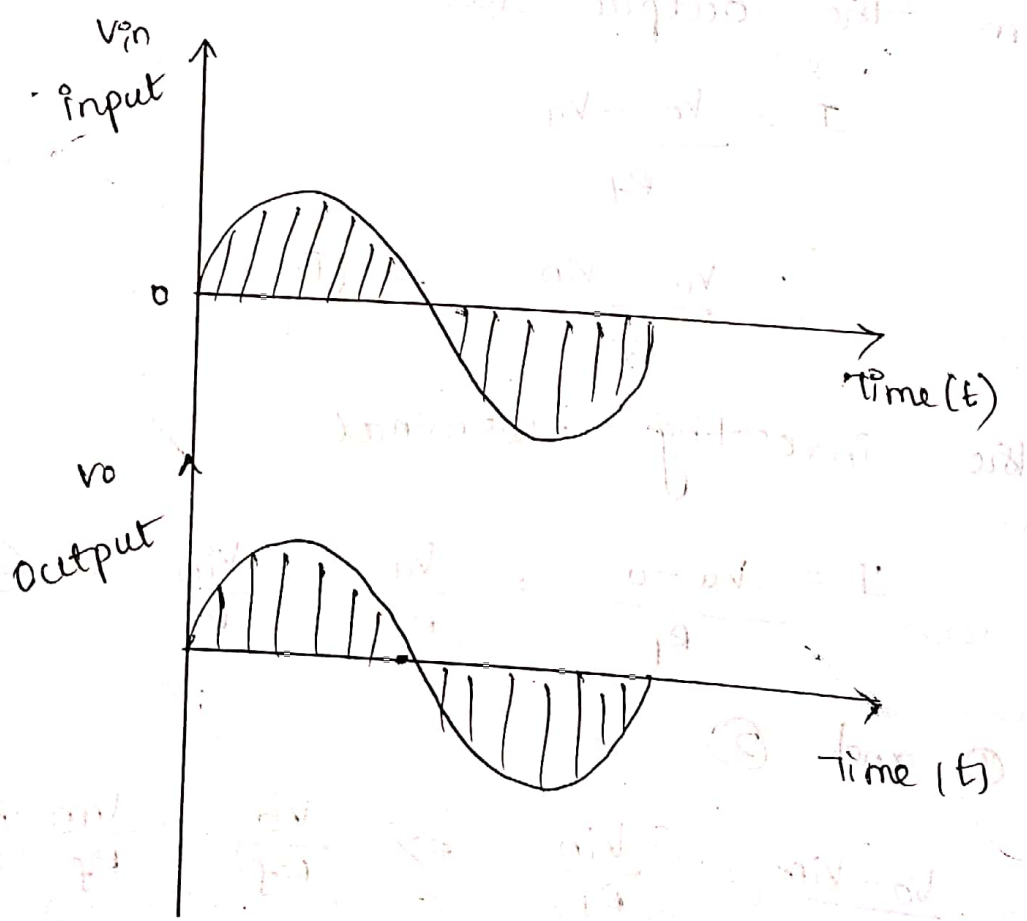


Fig 2.4.2 waveforms of non inverting amplifier

2.4.1 Comparison

Inverting amplifier	Non inverting amplifier
1. voltage gain = $-R_f/R_1$	voltage gain = $1+(R_f/R_1)$
2. The output is inverted with respect to input.	No phase shift between input and output.
3. The voltage gain can be adjusted as greater than, equal or less than one.	The voltage gain is always greater than one.
4. The input impedance is R_1.	The input impedance is extremely large.

2.2 Realistic simplifying Assumptions:

We can make two assumptions which are realistic and simplify the analysis of op-amp circuits to a great extent. The assumptions are useful and can be used to obtain the output expressions in variety of linear applications.

1) Zero input current
2) Virtual ground.

2.2.1 Zero Input current:

The current drawn by either of the input terminals (inverting and non inverting) is zero.

In practice, the current drawn by the input terminals is very small, of the order of μA or nA. Hence the assumption of zero input current is realistic.

2.2.2 Virtual ground :

This means the differential input voltage V_d between the non inverting and inverting input terminals is essentially zero.

If output voltage is 10V and open loop gain A_{OL} is 10^4 then

$$V_o = A_d V_d \Rightarrow V_o = A_{OL} V_d$$

$$V_d = \frac{V_o}{A_{OL}} = \frac{10}{10^4} = 1\,mV.$$

Hence V_d is very small, As $A_{OL} \to \infty$ the difference voltage $V_d = 0$ and realistically assumed to be zero for analysing the circuits.

$$V_d = \frac{V_o}{A_{OL}} \quad (i.e) \quad V_1 - V_2 = \frac{V_o}{\infty} = 0$$

$$V_1 - V_2 = 0$$

$$\Rightarrow V_1 = V_2$$

Thus we can say that under linear range of operation there is virtually short circuit between the two input terminals, in the sense that their voltages are same.

no current flows from the input terminals to the ground.

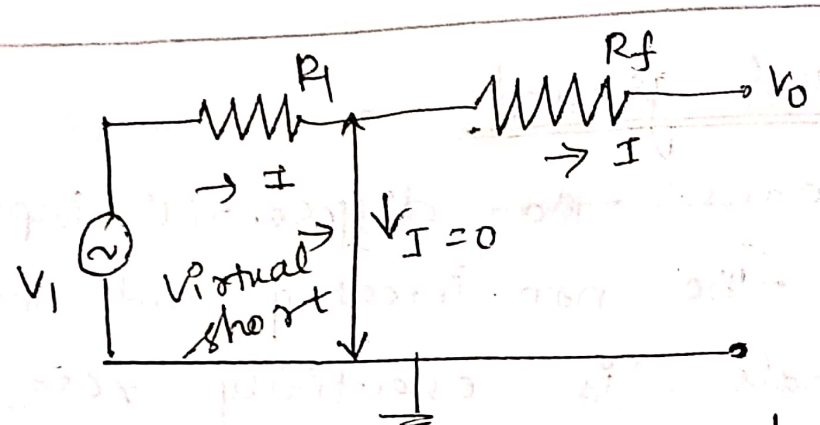


Fig 2.2.1 Concept of virtual ground in op-amp.

If the non inverting terminal is grounded, by the concept of virtual ground, the inverting terminal is also at ground Potential, though there is no physical connection between the inverting terminal and the ground.

This is the principle of virtual ground.

2.3 Inverting amplifier :-

help of transistors is preferred which has no effect on the output voltage swing under short circuit condition.

1.8 Practical op-amp characteristics :-

The characteristics of an ideal op-amp can be approximated closely enough, for many practical op-amps.

But basically the practical op-amp characteristics are little bit different than the ideal op-amp characteristics.

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1) Open loop gain :-

It is the voltage gain of the op-amp when no feedback is applied. practical it is several thousands.

2) Input impedance :-

It is finite and typically greater than 1MΩ. But using FETs for the input stage, it can be increased upto several hundred MΩ.

3) output impedance :-

It is typically few hundred ohms. with the help of negative feedback it can be reduced to a very small value like 1 or 2 ohms.

4) Bandwidth :-

The Bandwidth of practical op-amp in open loop configuration is very small. By application of negative feedback, it can be increased to a desired value.

The range of frequency over which the amplifies performance is satisfactory is called its Bandwidth.

5) Input offset voltage :-

Whenever both the input terminals of the

op-amp are grounded, ideally the output voltage should be zero.

In this condition, the practical op-amp shows a small non zero output voltage. To make this voltage zero, a small voltage in millivolts is required to be applied to one of the input terminals. Such a voltage makes the output exactly zero.

This d.c voltage, which makes the output voltage zero, when the other terminal is grounded is called input offset voltage. It is denoted as V_{ios}.

6) Input bias current:

The average value of the two currents flows into the op-amp input terminals is called input bias current and denoted as I_b.

$$I_b = \frac{|I_{b1}| + |I_{b2}|}{2}$$

maximum value of I_b is 500 nA.

7) Input offset current:

The algebraic difference between the currents flowing into the two input terminals of the opamp is called input offset current denoted as I_{ios}.

$$I_{ios} = |I_{b1} - I_{b2}|$$

I_{b1} = current entering into the non inverting input terminal

I_{b2} = current entering into inverting input terminal.

Ideally I_{os} is zero while for op-amp maximum value of I_{os} is 200nA.

8) Output offset voltage (V_{oos})

The d.c voltage present at the output terminals when both the input terminals are grounded is called output offset voltage denoted as V_{oos}.

V_{oos} = V_o due to I_b + V_o due to V_{ios}.

1.9 Other Important Op-amp parameters.

1) slew rate
2) power supply rejection ratio (PSRR)

1) Power supply rejection ratio (PSRR)

The power supply rejection ratio (PSRR) is defined as the ratio of the change in input offset voltage due to the change in supply voltage producing it, keeping other power supply voltage constant. It is also called power supply sensitivity (PSV)

$$PSRR = \left.\frac{\Delta V_{ios}}{\Delta V_{cc}}\right|_{\text{constant } V_{EE}}$$

For a fixed V_{cc}, if there is a change in V_{EE} then

$$PSRR = \left.\frac{\Delta V_{ios}}{\Delta V_{EE}}\right|_{\text{Constant } V_{cc}}$$

PSRR is expressed in mV/V or μV/V. The typical value of PSRR for IC741 opamp is 30 μV/V.

2) Slew rate :

The slew rate is defined as the maximum rate of change of output voltage with time. The slew rate is specified in V/μsec.

$$\text{slew rate} = S = \left.\frac{dv_o}{dt}\right|_{max}$$

1.10 D.C characteristics of op-amp :

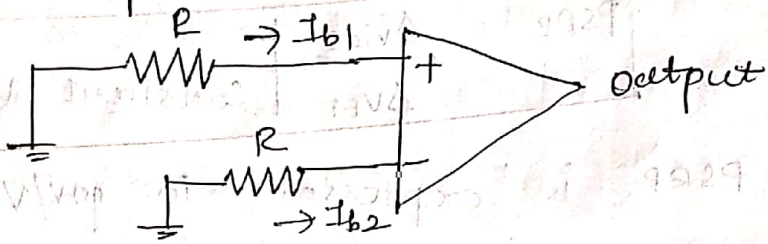
The important d.c characteristics of op-amp are

1. Input bias current (I_b)
2. Input offset current (I_{ios})
3. Input offset voltage (V_{ios})
4. Thermal drift.

Integrated

1.10. 1) Input bias current :-

The average value of the two currents flowing into the op-amp input terminals is called input bias current and denoted I_b



Mathematically it is expressed as

$$I_b = \frac{|I_{b1}| + |I_{b2}|}{2}$$

Ideally it should be zero while for op-amp 741C, maximum value of I_b is 500 nA. BJT, FET 50 pA

1.10. 2) Input offset current :-

It is seen that the input stage of the op-amp is the dual input differential amplifier and the input terminals are the base terminals of the two transistors.

Hence the input currents of op-amp are the base currents of the two transistors Q_1 and Q_2 used in the input stage.

Ideally Q_1 and Q_2 must be perfectly

matched and two base currents differs by small amount.

The algebraic difference between the currents flowing into the two input terminals of the op-amp is called is called Input offset current and denoted as I_{ios}.

Mathematically it is expressed as

$$I_{ios} = |I_{b1} - I_{b2}|$$

Ideally I_{ios} is zero while for op-amp 741C maximum value of I_{ios} is 200 nA.

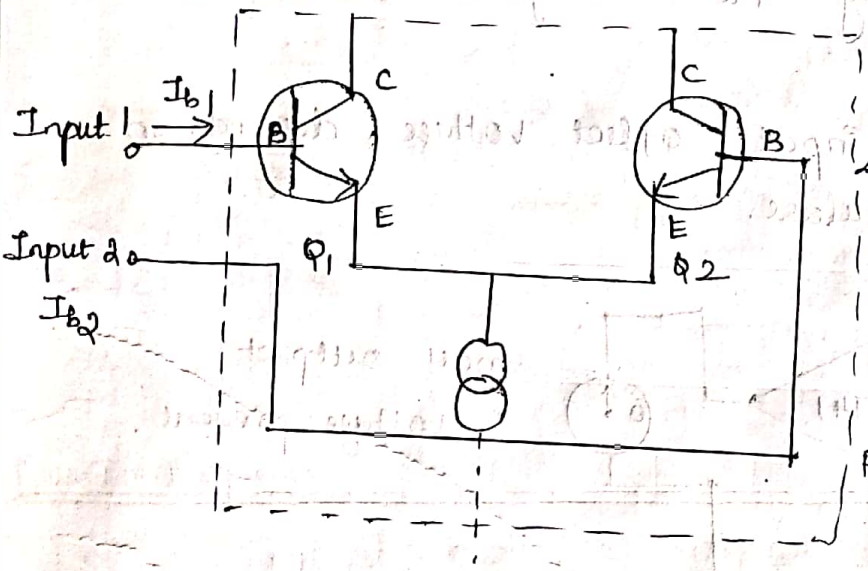


Fig: 1.10.1 Input offset current

1.10.3) Input offset voltage :

Whenever both the input terminals of the op-amp are grounded, ideally the output voltage should be zero.

However in this condition, the practical op-amp shows a small non zero output voltage. To make this output voltage zero,

a small voltage in millivolts is required to be applied to one of the input terminals.

Such a voltage makes the output exactly zero.

This d.c voltage, makes the output voltage zero, when the other terminal is grounded is called input offset voltage denoted as Vios.

How much voltage, to which terminal and with what polarity to be applied is specified by the manufacturer in the datasheet.

The input offset voltage depends on the temperature.

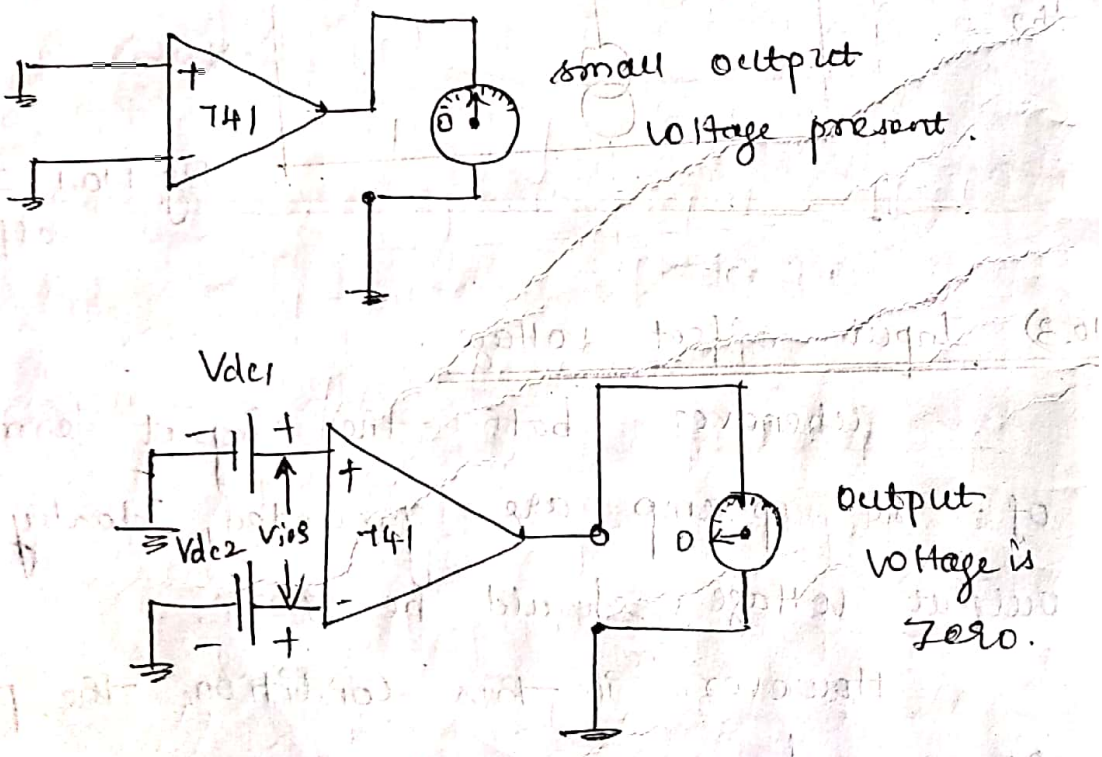


Fig 1.10.2 Concept of input offset voltage.

$$V_{IOS} = |V_{dc1} - V_{dc2}|$$

The V_{IOS} can be positive or negative hence absolute value of the V_{IOS} is mentioned in the data sheet.

The smaller value of V_{IOS}, better the matching of input terminals.

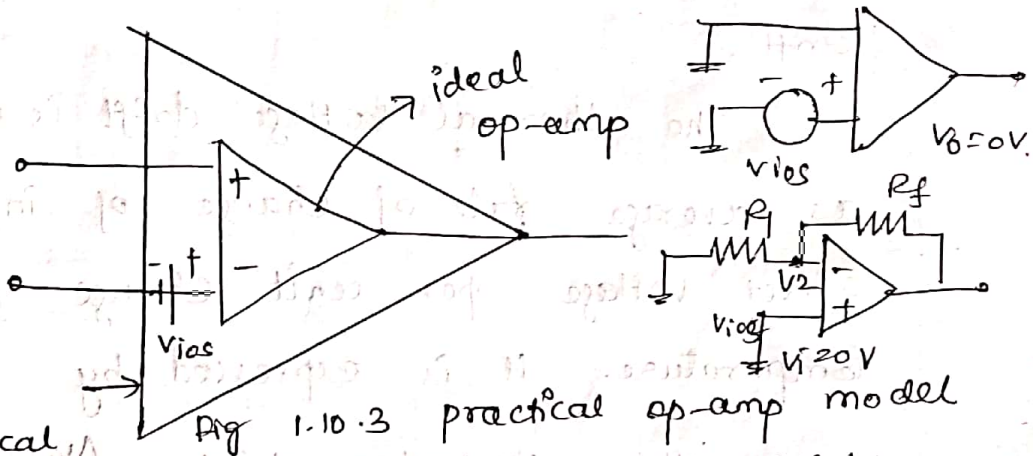


Fig 1.10.3 practical op-amp model with V_{IOS}.

$V_{IOS} = |0 - V_2| = V_2 \Rightarrow V_0 = \left(1 + \frac{R_f}{R_1}\right) V_{IOS}$.

For ideal op-amp V_{IOS} is zero, For op-amp 741C the input offset voltage is 6mV.

1.10.4) Thermal drift :-

The op-amp parameters input offset voltage V_{IOS}, Input bias current I_B and Input offset current I_{IOS} are not constants but vary with the factors

i) Temperature
ii) Supply voltage changes
iii) Time

Let us discuss the effect of change in temperature on these parameters.

1.10.4.1 Effect on Input offset voltage :-

The effect of change in temperature on the input offset voltage is defined by a factor called thermal voltage drift. It is also called as input offset voltage drift.

The thermal voltage drift is defined as average rate of change of input offset voltage per unit change in temperature. It is expressed by —

$$\text{thermal voltage drift} = \frac{\Delta V_{IOS}}{\Delta T}$$

It is expressed in μV/°c. The drift is not constant and it is not uniform over specified operating temperature range.

The value of the input offset voltage may increase or decrease with the increasing temperature.

The figure shows the graph of normalized values of input offset voltage versus temperature.

The input offset voltage is zero at room temperature of 25°c.

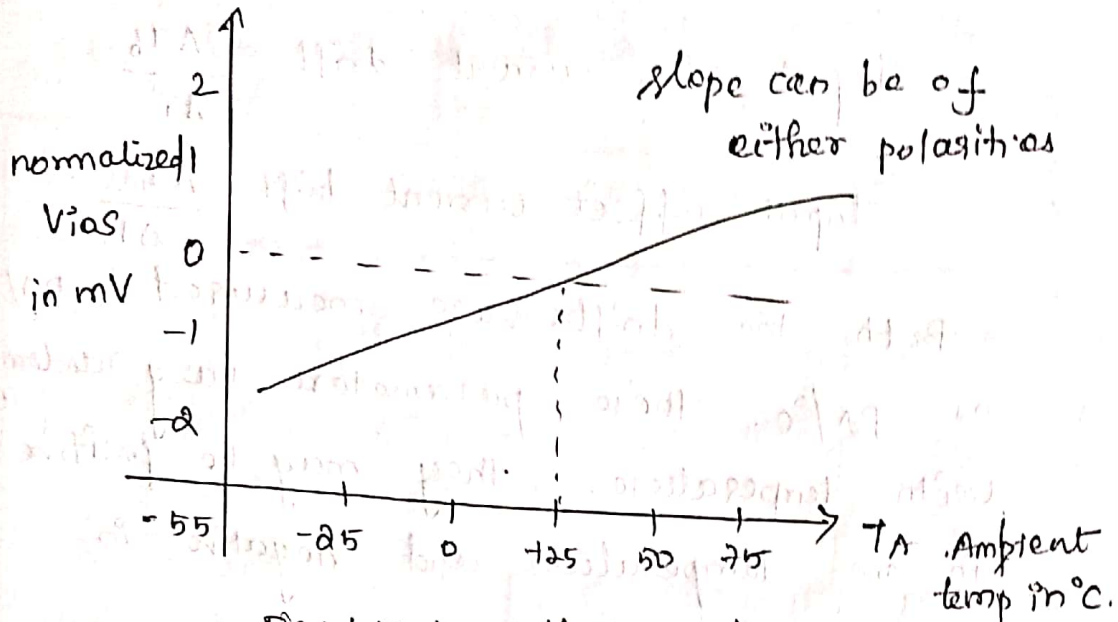


Fig: 1.10.4 Effect on input offset voltage

1.10.2 Effect on Input offset and Bias currents :-

Similar to the input offset voltage, input bias current and Input offset current are not constants but vary with temperature.

The effect of temperature on input bias current is defined by a factor called input bias current drift while offset or input offset current is defined by a factor called input offset current drift.

The average rate of change of input bias current per unit change in temperature is called input bias current drift.

The average rate of input offset current per unit change in temperature is called input offset current drift.

Input bias current drift = $\frac{\Delta I_b}{\Delta T}$.

Input offset current drift = $\frac{\Delta I_{ios}}{\Delta T}$.

Both the drifts are measured in nA/°C or pA/°C. These parameters vary randomly with temperature. They may be positive in one temperature and negative in another.

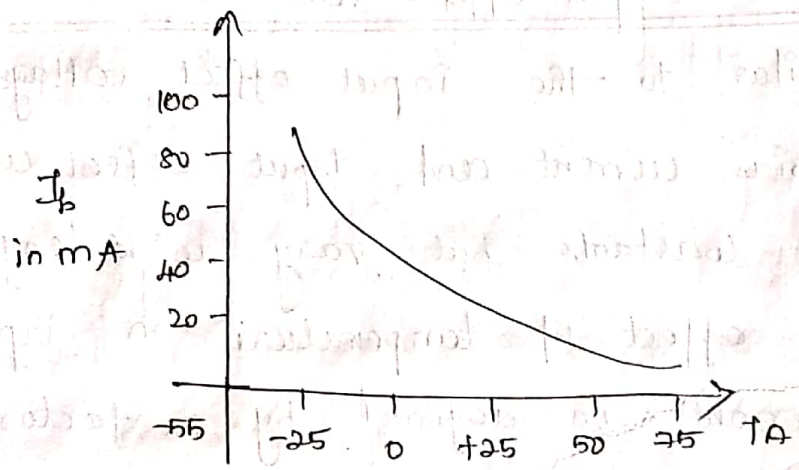


Fig. 1.10.5 Input bias current drift.

Figure shows the graphs of normalized values of input bias current and input offset current versus temperature for MC1741 op-amp.

These curves are different for different types of op-amps and are generally provided by the manufacturers.

Ideal Vs practical characteristics of IC741 opamp.

S.no	parameter	Symbol	Ideal	For 741 IC
1.	open loop voltage gain	AOL	∞	2×10^5
2.	output impedance	Zout	0	75Ω
3.	Input impedance	Zio	∞	2MΩ
4.	Input offset current	Iios	0	20nA
5.	Input offset voltage	Vios	0	2mV
6.	Bandwidth	BW	∞	1MHz
7.	CMRR	ℓ	∞	90dB
8.	Slew rate	$\frac{}{}$	∞	0.5V/μsec
9.	Input bias current	I_b	0	80nA
10.	power supply rejection ratio	PSRR	0	30μV/V.

Table 1.10.1 Ideal Vs practical characteristics of IC741opamp.

1.11 AC characteristics of opamp :-

The important a.c characteristics of op-amp are

1. slew rate
2. Frequency response.
3. Bandwidth

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1.11.1 Frequency response of op-amp:

Ideally an op-amp should have an infinite bandwidth. This means the gain of op-amp must remain same for all the frequencies from zero to infinite.

Uptill now we have assumed gain of the op-amp as constant but practically op-amp gain decreases at higher frequencies. Such a gain reduction with respect to frequency is called roll off.

This happens because gain of the op-amp depends on the frequency and hence mathematically it is a complex number. Its magnitude and phase angle changes with the frequency.

The plot showing the variations in magnitude and phase angle of the gain due to the change in frequency is called frequency response of the op-amp.

When the gain in decibels, phase angle in degrees are plotted against logarithmic scale of frequency, the plot

is called Bode plot.

The manner in which the gain of the op-amp changes with variation in frequency is known as the magnitude plot and

the manner in which the phase shift changes with variation in frequency is known as the phase angle plot.

To obtain the frequency response, Consider the high frequency model of the op-amp with a capacitor C at the output taking into account the capacitive effect present.

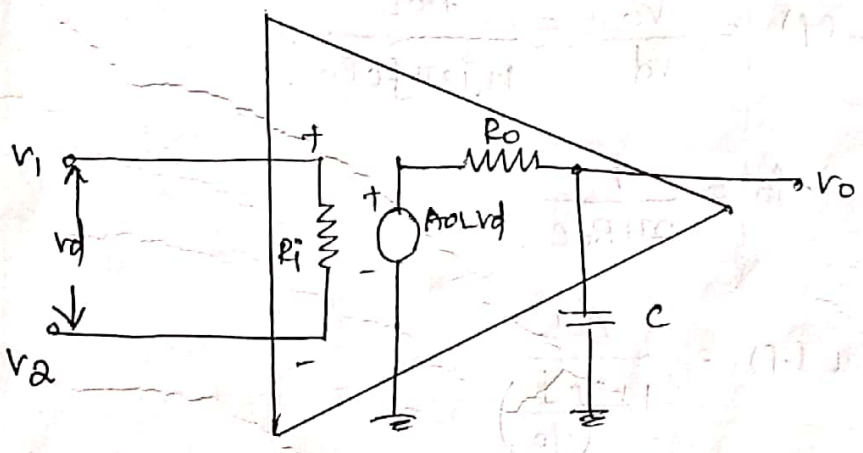

Fig: 1.11.1 high frequency model of the op-amp.

Let $-jX_C$ be the capacitance reactance due to the capacitor C.

$$V_o = -jX_c \left[\frac{A_{OL} V_d}{R_o - jX_c} \right]$$

$-j = \frac{1}{j}$ and $X_c = \frac{1}{2\pi f c}$.

$$V_o = \frac{\frac{1}{j2\pi f c}}{R_o + \frac{1}{j2\pi f c}} (A_{OL} V_d)$$

$$V_o = \frac{A_{OL} V_d / j2\pi f c}{\frac{1 + j2\pi f c R_o}{j2\pi f c}}$$

$$V_o = \frac{A_{OL} V_d}{1 + j2\pi f c R_o}$$

Hence the open loop voltage gain as a function of frequency is

$$A_{OL}(f) = \frac{V_o}{V_d} = \frac{A_{OL}}{1 + j2\pi f c R_o}.$$

$$f_o = \frac{1}{2\pi R_o C}.$$

$$A_{OL}(f) = \frac{A_{OL}}{1 + j\left(\frac{f}{f_o}\right)}$$

where $A_{OL}(f)$ = open loop voltage gain as a function of frequency.

A_{OL} = Gain of opamp at 0Hz.

f = Operating frequency.

f_o = cut off frequency of op-amp.

In polar form it can be written as

$$|A_{OL}(f)| = \frac{A_{OL}}{\sqrt{1+\left(\frac{f}{f_0}\right)^2}}$$

$$\angle A_{OL}(f) = \phi(f) = -\tan^{-1}\left(\frac{f}{f_0}\right).$$

At $f=0$, $|A_{OL}(f)| = A_{OL}$, while $\phi(f) = 0^\circ$.

For IC741 op-amp $f_0 = 5Hz$ and the open loop gain 200000 we can calculate gain and phase shifts at various frequencies.

Frequency in Hz	$\lvert A_{OL}(f)\rvert$ in dB = $20\log \frac{A_{OL}}{\sqrt{1+\left(\frac{f}{f_0}\right)^2}}$ in dB	$\phi(f) = -\tan^{-1}\left(\frac{f}{f_0}\right)$ in degrees
0	106.02 dB	0°
5	103.01 dB	-45°
10	99.03 dB	-63.43°
100	79.98 dB	-87.13°
1000	60 dB	-89.71°
100×10^3	20 dB	-89.99°
1×10^6	0 dB	-89.999°

Table. 1.11.1 Gain & Phase shifts at various frequencies

The following observations can be made from the frequency response of an op-amp.

1) The open loop gain A_{OL} is almost constant from 0Hz to the break frequency f_0.

2) At $f = f_0$, the gain is 3 dB down from its value at 0 Hz. Hence the frequency f_0 is also called as -3 dB frequency. It is also known as corner frequency.

3) After $f = f_0$, the gain $A_{OL}(f)$ decreases at a rate of 20 dB / decade. As gain decreases, slope of the magnitude plot is -20 dB / decade.

4) After a certain frequency, the gain reduces to 0 dB. This means $20 \log |A_{OL}(f)|$ is 0 dB. (ie) $|A_{OL}(f)| = 1$. Such a frequency is called gain cross-over frequency or unity gain bandwidth (UGB).

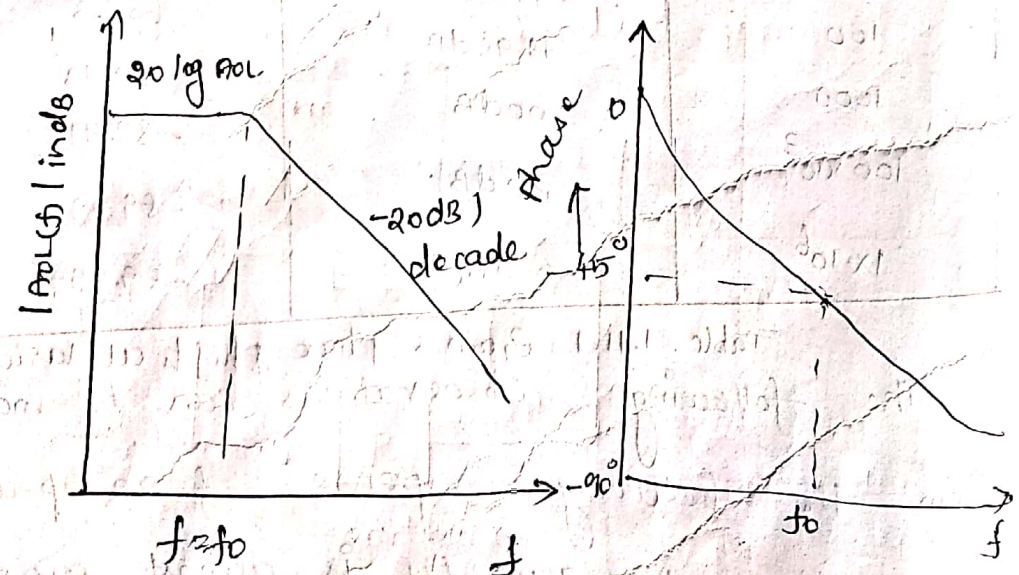

Fig. 1.1.2 magnitude characteristics

Fig: 1.1.3 phase characteristics

UGB is also called gain bandwidth product and denoted as ft. Thus ft is product of gain of op-amp and bandwidth.

The break frequency is nothing but a corner frequency fo.

The op-amp for which there is only one change in the slope of the magnitude plot is called as single break frequency op-amp.

For a single break frequency we can write

$$UGB = A_f f_f .$$

A_f → closed loop voltage gain

f_f → Bandwidth with feedback.

5) the phase angle of an op-amp with a single break frequency varies between 0° to 90°. the maximum possible phase shift is -90°.

6) At a corner frequency $f = f_o$, the phase shift is -45°.

1.11.5 Bandwidth :-

The Bandwidth of an amplifier is defined as the range of frequencies with in which the gain remains constant.

The gain - bandwidth product of an op-amp is always constant.

The gain of an op-amp and its bandwidth are inversely proportional to one another.

The bandwidth of an op-amp can be increased by providing feedback signal to its input.

The product of closed loop gain A_V and closed loop bandwidth BW_{CL} is same as the product of open-loop gain and open loop bandwidth. That is

$$A_V \times BW_{CL} = A_O \times BW_{OL}$$

$A_V \rightarrow$ Closed loop gain

$A_O \rightarrow$ open loop gain.

1.12 Slew rate:

Slew rate is defined as the maximum rate of change of output voltage with time. The rate is specified in V/μsec.

$$\text{Slew rate} = S = \left.\frac{dv_o}{dt}\right|_{max}$$

The slew rate of the op-amp is related to its frequency response. The op-amps with wide bandwidth have better slew rates.

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The general purpose op-amps such as the 741 have a maximum slew rate of 0.5V/μs which means that the output voltage can change at a maximum of 0.5V in 1 μs.

1.12 Causes of slew rate

The slew rate is determined by a number of factors such as

1) Amplifier gain.
2) Compensating capacitors
3) change in polarity of output voltage.

It is also a function of temperature and the slew rate generally reduces due to rise in temperature.

$$\text{Slew rate} = \frac{\text{output voltage change}}{\text{Time}}$$

$$= \left.\frac{dV_c}{dt}\right|_{max} \qquad I = C\frac{dV_c}{dt}$$

$$= \frac{I_{max}}{C} \qquad \Rightarrow \frac{dV_c}{dt} = \frac{I_{max}}{C}$$

1.12.2 Effect of slew rate :-

Consider a circuit using op-amp having unity gain. The output is same as input. If the input is square wave output has to be square wave. But it is observed for certain frequency of input.

Due to slew rate of an op-amp for a particular input frequency, output gets distorted.

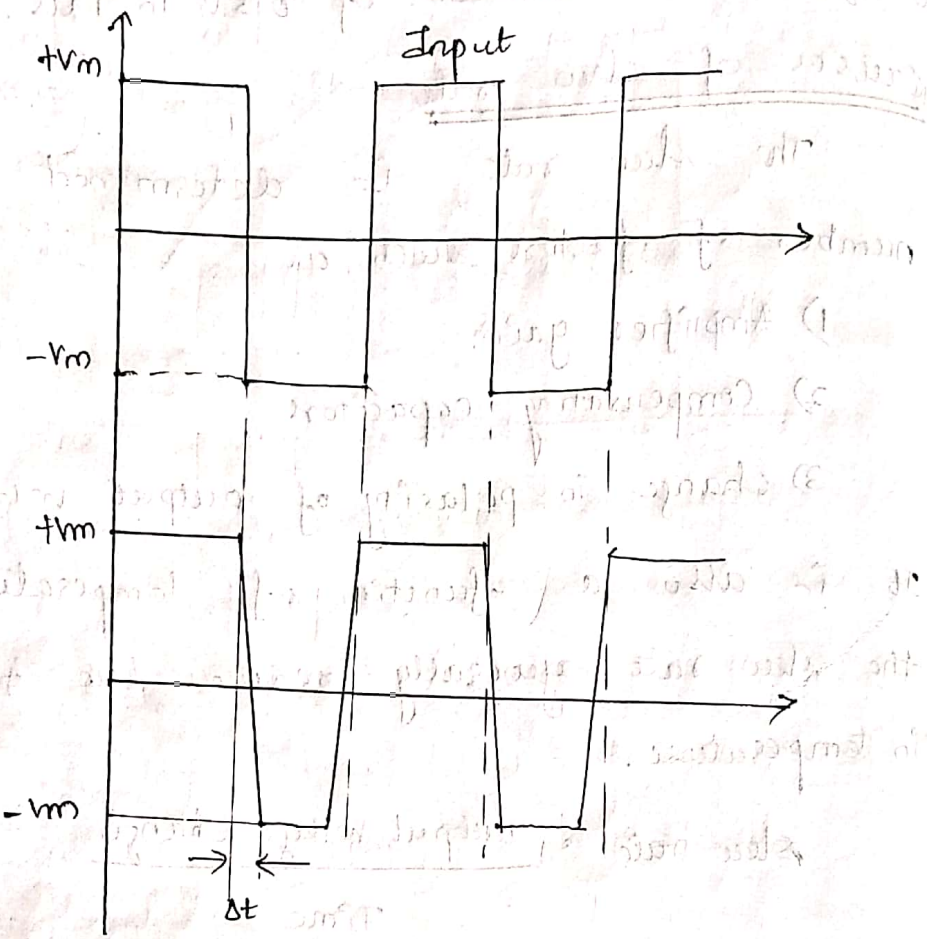


Fig 1.12.1 Effect of slew rate

1.12.3 slew rate equation:-

$$S = \frac{\Delta v_o}{\Delta t} \text{ V/sec}$$

Consider unity gain op-amp circuit with purely sinusoidal input. The output must be same as input.

$$v_i = V_m \sin \omega t$$

$$v_o = V_m \sin \omega t.$$

$$\frac{dv_o}{dt} = V_m \omega \cos \omega t \quad \text{— (1)}$$

$$S = \text{Slew rate} = \left.\frac{dv_o}{dt}\right|_{max}$$

The equation (1) has maximum value when $\cos\omega t = 1$

$$S = V_m\omega = 2\pi f V_m$$

$$S = 2\pi f V_m \ V/\mu sec.$$

This is the required slew rate equation.

For distortion free output, the maximum allowable input frequency f_m can be obtained as

$$f_m = \frac{S}{2\pi V_m} \ Hz.$$

This is also called full power bandwidth of the op-amp. The V_m is peak of output waveforms.

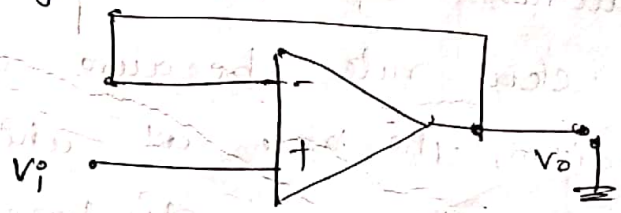


Fig 1.12.2 Unity gain op-amp or voltage follower.

1.12.4 Methods of improving slew rate :-

The slew rate is given by

$$S = \frac{I_{max}}{C}$$

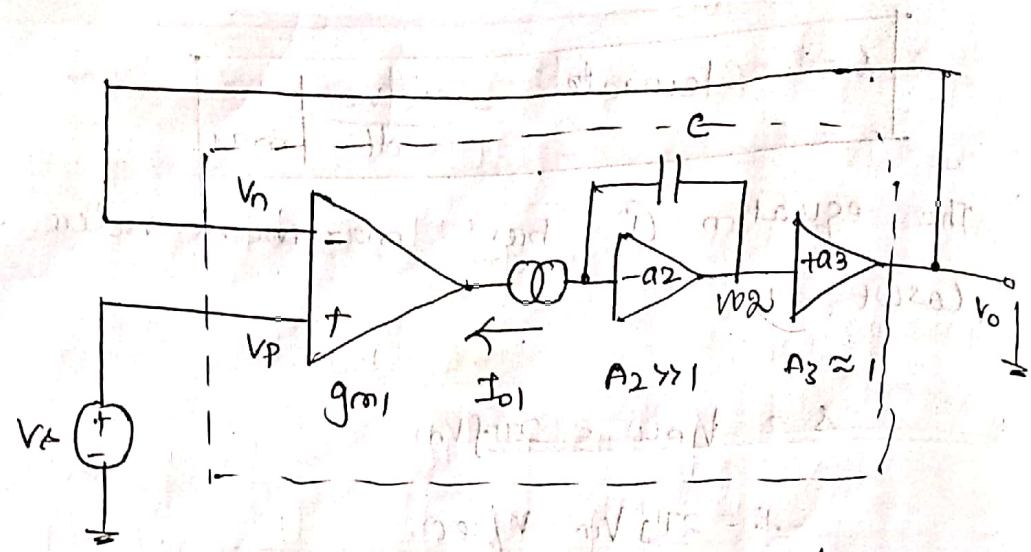


Fig 1.12.3 Op-amp model for slew rate analysis

The op-amp used is in voltage follower mode, in which the output voltage follows the input voltage. that is (i.e) $V_o = V_i$.

when input overdrives the input stage then $I_{max} = \pm I_{o1}(sat)$ which are saturation current levels of the input stage.

The saturation of the input stage limits the slew rate because under saturation condition, the rate at which capacitor C can charge or discharge, according to the input overdrive is at its maximum.

$$I_{o1}(Sat) = \frac{C\, d v_{o2}}{dt}$$

(ie) $$\frac{d v_{o2}}{dt} = \pm \frac{I_{o1}(sat)}{C}$$

the gain of third stage $a_3 \approx 1$ hence $v_o = v_{o2}$

$$\left.\frac{dv_o}{dt}\right|_{max} = \frac{dv_{o2}}{dt} = \frac{I_{o1}(sat)}{C}.$$

Slew rate $(s) = \frac{I_{o1}(sat)}{C}$.

Analysing the op-amp model used we can write

v_{o2} = drop across C = $Z_C I_{o1}$.

The input stage is a trans conductance amplifier. (ie) voltage input, current output amplifier.

output current = g_m (differential input)

$$I_{o1} = g_{m1}(V_p - V_n)$$

$$V_{o2} = Z_C I_{o1}$$

$$= Z_C g_{m1}(V_p - V_n)$$

$V_{o2} = V_o$ as $a_3 \approx 1$

$$V_o = Z_C g_{m1}(V_p - V_n)$$

$$Z_C = \frac{1}{j\omega C}$$

$$V_o = \left[\frac{1}{j\omega C}\right] g_{m1}(V_p - V_n).$$

$$\therefore \text{Op amp gain} = \frac{|V_o|}{|V_p - V_n|} = \left|\frac{V_o}{V_p - V_n}\right| = \frac{g_{m1}}{\omega C}$$

$$C = \frac{g_{m1}}{2\pi f C}$$

$$|a| f = \frac{g_{m1}}{2\pi C}$$

The gain bandwidth product of op-amp is denoted as f_t given by the product of gain $|a|$ and bandwidth f as,

$$f_t = |a| f$$

$$\text{(ie)} \quad f_t = \frac{g_{m1}}{2\pi C}$$

$$C = \frac{g_{m1}}{2\pi f_t}$$

The gain bandwidth product is also called unity gain bandwidth of op-amp.

Substituting value of C in slew rate.

$$S = \frac{I_{D1}(sat)}{C}$$

$$= \frac{I_{D1}(sat)}{\frac{g_{m1}}{2\pi f_t}}$$

$$\boxed{S = \frac{2\pi I_{D1}(sat)}{g_{m1}} f_t}$$

From this equation, we get an idea about improvement in slew rate.

Methods of improving slew rate are

1) Increasing f_t

2) Increasing $I_{01}(sat)$

3) Reducing g_{m1}.

1.2 Current mirror and current sources :-

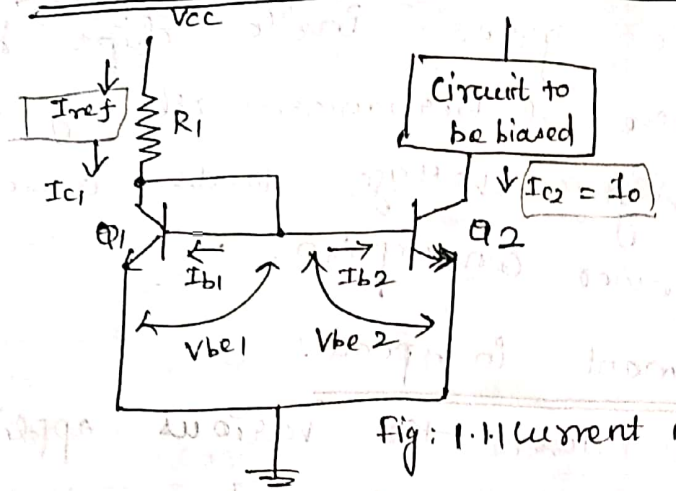
The circuit in which the output current is forced to equal to input current is called current mirror circuit.

In the current mirror circuit, the output current is the mirror image of input current.

A constant current source makes use of the fact that for a transistor in the active mode of operation.

The collector current is independent of the collector voltage.

Basic current mirror circuit



To prove Iref = Io

Iref = Ic2 = Io

fig: 1.1 Current mirror circuit

→ Transistors Q1 and Q2 are matched as the circuit is fabricated using IC technology.

The bases and emitter of Q1 and Q2 are tied together and thus have the same VBE.

The input current, Iref flows through the transistor Q1 and thus establishes a voltage across Q1. This voltage in turn appears between the base and emitter of Q2.

Since Q2 is identical to Q1, the emitter current of Q2 will be equal to emitter current of Q1 which is approximately equal to Iref.

We can say that as long as Q2 is maintained in the active region, its collector current Ic2 = Io will be approximately equal to Iref.

Since the o/p current I_o is a reflection or mirror of the reference current I_{ref}, the circuit is often referred to as a current mirror.

This mirror effect is valid only for large values of β.

Analysis:

The collector current I_{C1} and I_{C2} for transistors Q_1 and Q_2 can be approximately expressed as

$$I_{C1} = \alpha_F I_{ES} e^{V_{BE1}/V_T} \quad \text{—— (1)}$$

$$I_{C2} = \alpha_F I_{ES} e^{V_{BE2}/V_T} \quad \text{—— (2)}$$

From eqn (1) and eqn (2)

$$\frac{I_{C2}}{I_{C1}} = \frac{e^{V_{BE2}/V_T}}{e^{V_{BE1}/V_T}}$$

$$= e^{(V_{BE2} - V_{BE1})/V_T} \quad \text{—— (3)}$$

since $V_{BE1} = V_{BE2}$, $I_{C2} = I_{C1} = I_C = I_o$.

Also since both transistors are identical

$$\beta_1 = \beta_2 = \beta$$

KCL at the collector of Q_1 gives

$$I_{ref} = I_{C1} + I_{B1} + I_{B2}$$

$I_B = \frac{I_C}{\beta}$

I_B replaced by I_C ⇒

$$= I_{C1} + \frac{I_{C1}}{\beta_1} + \frac{I_{C2}}{\beta_2}$$

$I_{C1} = I_{C2}$ ⇒

$$= I_{C1}\left(1 + \frac{1}{\beta_1} + \frac{1}{\beta_2}\right)$$

$$\beta_1 = \beta_2 = \beta$$

$$I_{ref} = I_{C_1}\left(1 + \frac{1}{\beta} + \frac{1}{\beta}\right)$$

$$= I_C\left(\frac{\beta + 1 + 1}{\beta}\right)$$

$$= I_C\left(\frac{2+\beta}{\beta}\right)$$

$$\boxed{I_{ref} = I_C\left(1 + \frac{2}{\beta}\right)} \quad \text{---} \quad (4)$$

From eqn (4)

$$I_C = \frac{I_{ref}}{\left(1 + \frac{2}{\beta}\right)}$$

$$I_C = \frac{I_{ref}}{\left(\frac{\beta+2}{\beta}\right)}$$

$$\boxed{I_C = I_{ref}\left(\frac{\beta}{\beta+2}\right)} \quad \text{---} \quad (5)$$

We know that $\boxed{I_C = I_{ref}}$

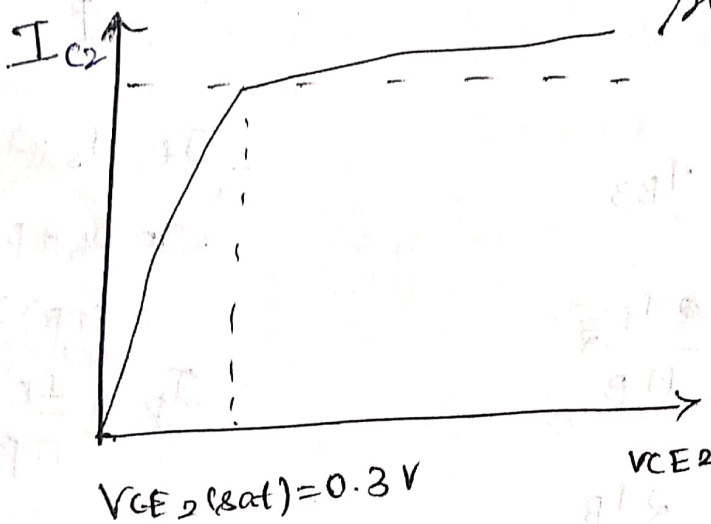
$$I_{ref} = \frac{V_{CC} - V_{BE}}{R_1} = \frac{V_{CC}}{R_1}$$ $V_{BE} = 0.7V$ is small

From eqn (5) for $\beta >> 1$ $\frac{\beta}{\beta+2}$ is almost unity

The O/P current I_o is equal to the reference current I_{ref}, which for a given R_1 & V_{CC} is constant.

The circuit operates as a constant current source as long as Q_2 remains in the active region.

The VI characteristics of Q2 is shown.



Current source is an electronic circuit that delivers or absorbs an electric current which is independent of the voltage across it.

2.2 Widlar current source circuit :

The basic current mirror circuit has a limitation. Whenever, we need low value current source, the value of the resistance R1 required is sufficiently high and cannot be fabricated economically in IC circuits.

Widlar current source is particularly

suitable for low value of currents.

The circuit differs from the basic current mirror only in the resistance R_E that is included in the emitter lead of Q_2.

It can be seen that due to R_E, the base emitter voltage V_{BE_2} is less than V_{BE_1} and consequently current I_o is smaller than I_{C1}.

We know that

$$I_{C_1} = \alpha_F I_{ES} e^{V_{BE_1}/V_T}$$

$$I_{C_2} = \alpha_F I_{ES} e^{V_{BE_2}/V_T}$$

The ratio of collector currents I_{C_1} and I_{C_2}.

$$\frac{I_{C_1}}{I_{C_2}} = e^{(V_{BE_1} - V_{BE_2})/V_T}$$

Taking natural logarithm of both sides, we get

$$V_{BE_1} - V_{BE_2} = V_T \ln\left(\frac{I_{C_1}}{I_{C_2}}\right) \quad \text{——(1)}$$

writing KVL for the emitter base loop.

$$V_{BE_1} - V_{BE_2} - [(I_{B_2} + I_{C_2})]R_E = 0.$$

$$V_{BE_1} = V_{BE_2} + [(I_{B_2} + I_{C_2})]R_E$$

$$= V_{BE_2} + \left[\left(\frac{I_{C_2}}{\beta} + I_{C_2}\right)\right]R_E$$

$$= V_{BE_2} + [I_{C_2}]R_E\left(\frac{1}{\beta} + 1\right)$$

$$V_{BE_1} - V_{BE_2} = [I_{C_2}]R_E\left(\frac{1}{\beta} + 1\right) \quad \text{——(2)}$$

From (1) and (2)

Widlar current source circuit.

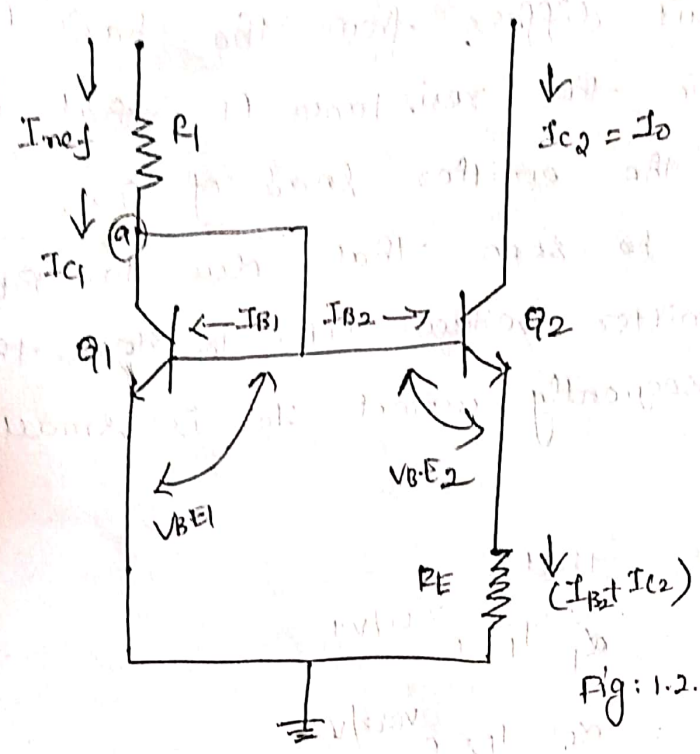


Fig: 1.2.2 widlar current source circuit

$$\left(\frac{1}{\beta}+1\right) I_{C2} R_E = V_T \ln \frac{I_{C1}}{I_{C2}}$$

$$R_E = \frac{V_T \ln \frac{I_{C1}}{I_{C2}}}{\left(\frac{1}{\beta}+1\right) I_{C2}}$$

writing KCL at node a

$$I_{ref} = I_{C1} + I_{B1} + I_{B2}$$

$$= I_{C1} + \frac{I_{C1}}{\beta} + \frac{I_{C2}}{\beta}$$

$$I_{ref} = I_{C1}\left(1 + \frac{1}{\beta}\right) + \frac{I_{C2}}{\beta} \quad \text{— (3)}$$

$$\left[\because \beta_2 = \beta_1 = \beta\right]$$

In the widlar current source $I_{C2} << I_{C1}$ therefore the term $\frac{I_{C2}}{\beta}$ may be neglected in eqn (3).

$$\therefore I_{ref} = I_{C1}\left(1 + \frac{1}{\beta}\right)$$

$$\Rightarrow I_{C1} = \frac{I_{ref}}{\left(1+\frac{1}{\beta}\right)} = \frac{I_{ref}}{\frac{\beta+1}{\beta}}$$

$$I_{C1} = I_{ref} \frac{\beta}{\beta + 1}$$

where $I_{ref} = \frac{V_{CC} - V_{BE}}{R_1}$

for $\beta \gg 1$ $\quad \boxed{I_{C1} = I_{ref}}$

By using widlar current source circuit we can use relatively small resistors to generate small currents.

4 Wilson current source :-

In wilson current source, the o/p current I_o, which is very nearly equal to I_{ref} and also exhibits a very high output resistance.

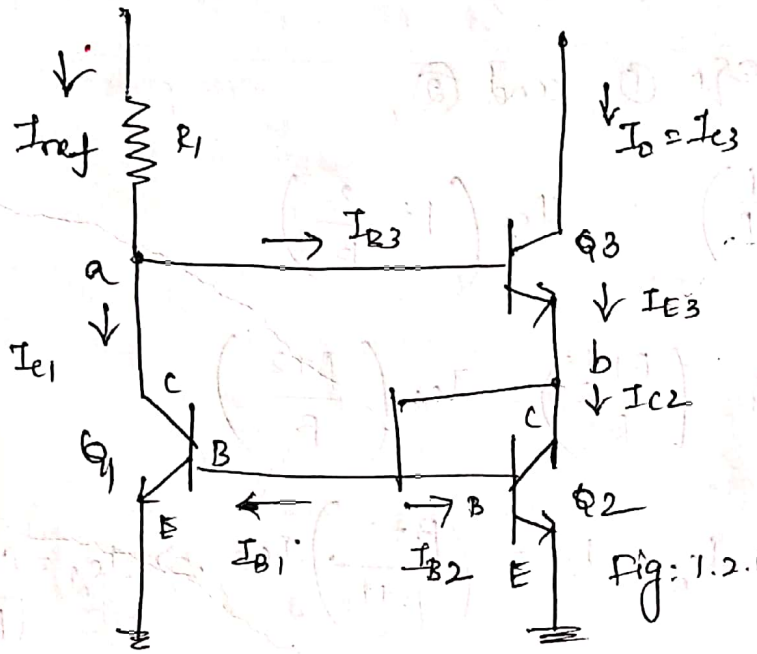


Fig: 1.2.4 wilson current source.

$V_{BE1} = V_{BE2}$, $I_{C1} = I_{C2}$ and $I_{B1} = I_{B2} = I_B$

At node b

$$I_{E3} = 2I_B + I_{C2}$$

$$= 2\frac{I_{C2}}{\beta} + I_{C2}$$

$$I_{E3} = \left(\frac{2}{\beta} + 1\right) I_{C2} \quad \text{——— (1)}$$

I_{E3} is also equal to

$$I_{E3} = I_{C3} + I_{B3}$$

$$= I_{C3} + \frac{I_{C3}}{\beta}$$

$$I_{E3} = I_{C3}\left(1 + \frac{1}{\beta}\right) \quad \text{——— (2)}$$

$$I_{E3} = I_{C2} + I_{B1} + I_{B2}$$

$$= I_{C2} + \frac{I_{C1}}{\beta} + \frac{I_{C2}}{\beta}$$

$$= I_{C2} + \frac{I_{C2}}{\beta} + \frac{I_{C2}}{\beta}$$

$$= I_{C2}\left(1 + \frac{2}{\beta}\right)$$

$$I_{E3} = I_{C2}\left(1 + \frac{2}{\beta}\right)$$

$$I_{E3} = I_{C3}\left(1 + \frac{1}{\beta}\right)$$

From eqn ① and ②

$$I_{C3}\left(1 + \frac{1}{\beta}\right) = I_{C2}\left(1 + \frac{2}{\beta}\right)$$

$$I_{C3}\left(\frac{\beta+1}{\beta}\right) = I_{C2}\left(\frac{\beta+2}{\beta}\right)$$

$$I_{C3} = I_0 = \left(\frac{\beta+2}{\beta+1}\right) I_{C2} \Rightarrow I_{C2} = \left(\frac{\beta+1}{\beta+2}\right) I_0$$

$\because I_{C1} = I_{C2}$

$$I_0 = \left(\frac{\beta+2}{\beta+1}\right) I_{C1}.$$

At node a.

$$I_{ref} = I_{C1} + I_{B3} \Rightarrow I_{C2} + I_{B3}$$

$$= \left(\frac{\beta+1}{\beta+2}\right) I_0 + \frac{I_{C3}}{\beta}$$

$$= \left(\frac{\beta+1}{\beta+2}\right) I_0 + \frac{I_0}{\beta} \qquad [I_{C3} = I_0]$$

$$= \left[\frac{\beta(\beta+1)+\beta+2}{\beta(\beta+2)}\right] I_0$$

$$= \left[\frac{\beta^2+\beta+\beta+2}{\beta^2+2\beta}\right] I_o$$

$$I_{ref} = \left[\frac{\beta^2+2\beta+2}{\beta^2+2\beta}\right] I_o$$

$$I_o = \frac{\beta^2+2\beta}{\beta^2+2\beta+2} I_{ref}.$$

where $I_{ref} = \frac{V_{cc} - 2V_{BE}}{R_1}$

$$\boxed{I_o \simeq I_{ref}}$$

2.5 Advantages of current mirror circuit :-

1) provides very high emitter resistance R_E
2) Requires less components. ~~tha~~
3) simple to design
4) Easy to fabricate
5) Thermal stability is achieved.

The constant current bias can be easily replaced by current mirror circuit to improve CMRR.

Due to its advantages, current mirror circuit is most commonly used in the integrated circuit op-amps.

2.10 Instrumentation Amplifier :-

In a number of industrial and consumer applications, one is required to measure and control physical quantities.

Some examples are measurement and control of temperature, humidity, light intensity water flow etc. These physical quantities are usually measured with the help of transducers.

A transducer is a device which converts one form of energy into another.

For example a thermocouple converts the heat energy into an electrical energy,

microphone converts the sound energy into electrical energy.

But most of the transducer outputs are generally of very low very signals. Such a low level signals are not sufficient to drive the next stage of the system.

Hence before the next stage, it is necessary to amplify the level of such signal, rejecting the noise and interference.

The special amplifier which is used for such a low level amplification with high CMRR, high input impedance, high gain accuracy, low power consumption, low output impedance is called an Instrumentation Amplifier.

Such a special featured instrumentation amplifiers have become a Integral part of modern testing and measurement Instrumentation.

It is also called data amplifier and it basically a difference amplifier. The expression for its voltage gain is

$$A = \frac{V_o}{V_2 - V_1}$$

$V_o \rightarrow$ o/p of the amplifier.

2.10.1 Requirements of good Instrumentation Amplifier:-

A good instrumentation amplifier has to meet the following specifications.

1) Finite, accurate and stable gain
2) Easier gain adjustment
3) High input impedance
4) Low output impedance
5) High CMRR
6) Low power consumption.
7) Low thermal and time drifts.
8) High slew rate.

2.10.2 Three op-amp Instrumentation amplifier

A commonly used Instrumentation amplifier circuit is one using three op-amps. This circuit provides high input resistance for accurate measurement of signals from transducers.

In this circuit, non inverting amplifier is added to each of the basic difference amplifier inputs.

The op-amp A_1 and A_2 are the non inverting amplifiers forming the input or first stage of the Instrumentation amplifier.

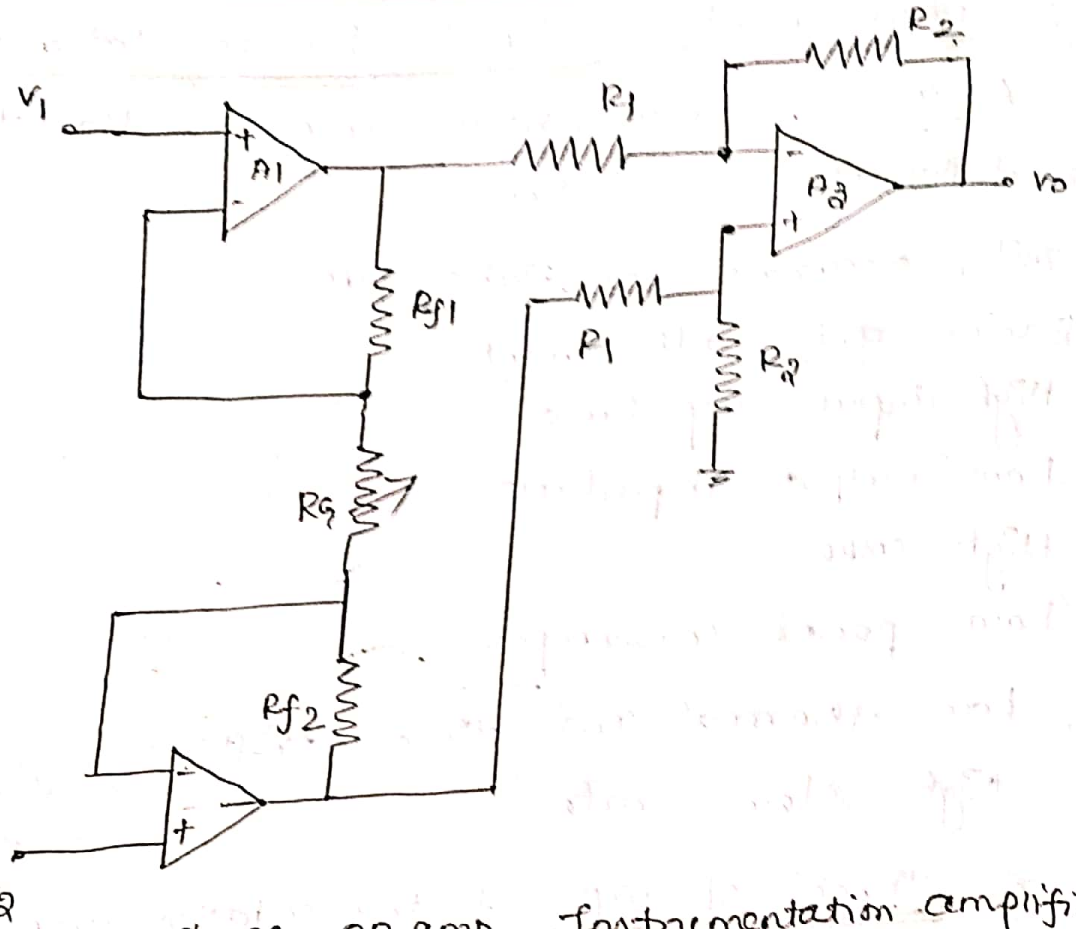
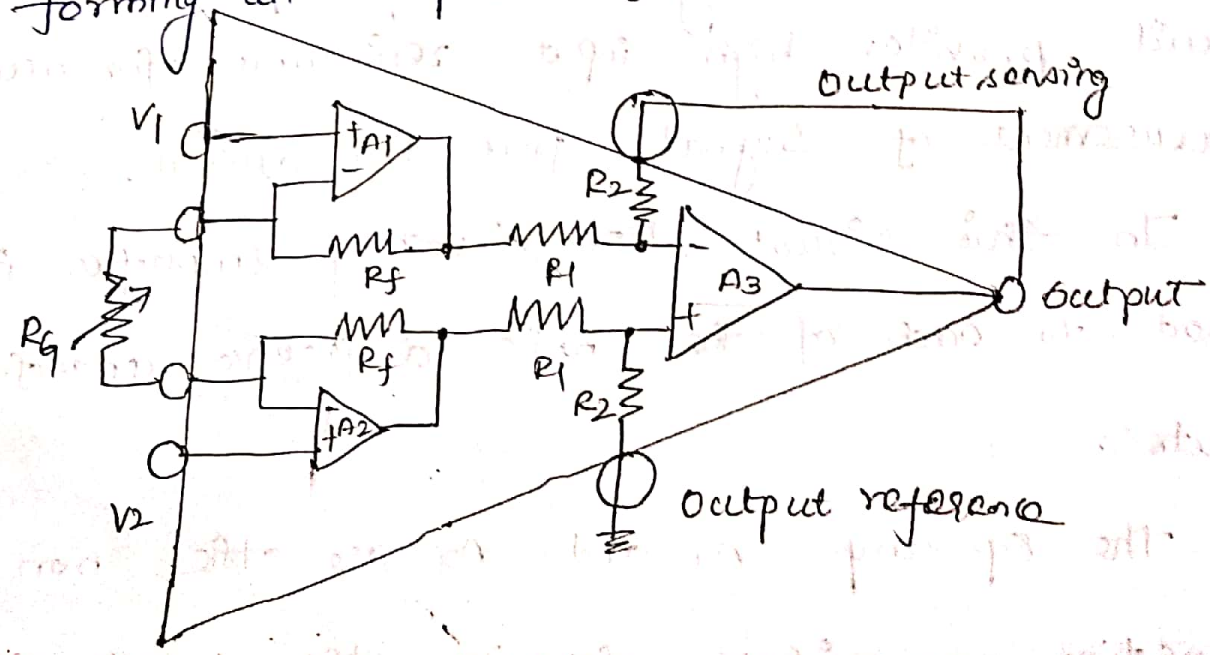


Fig 2.10.1 Three op-amp Instrumentation amplifies

The op-amp A_3 is the normal difference Amplifi forming an output stage of the amplifies.



2.10.2 Block diagram representation

2.10.3. Analysis of Three op-amp Instrumentation Amplifier:

The output state is a standard basic difference amplifier. so if the output of the op-amp A_1 is V_{o1} and the output of the opamp A_2 is V_{o2}, we can write

$$V_o = \frac{R_2}{R_1}(V_{o2} - V_{o1}).$$

Let us find out the expression for V_{o2} and V_{o1} interms of V_1, V_2, R_{f1}, R_{f2} and R_G.

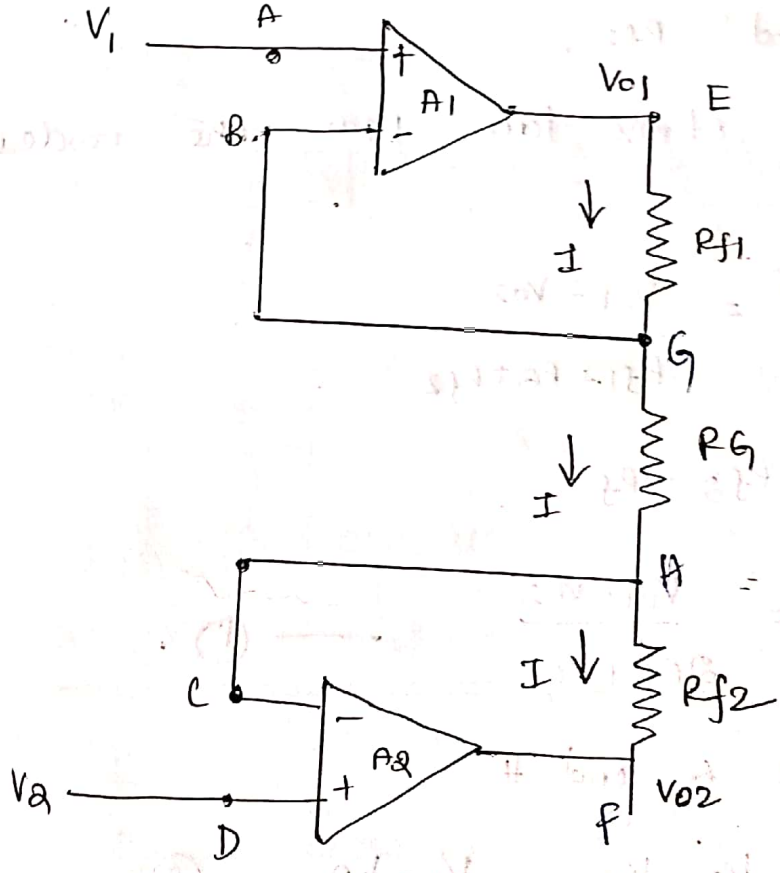


Fig 2.10.3 Analysis of Three op-amp Instrumentation amplifier

Consider the first stage as shown in figure.

The node A potential of op-amp A_1 is V_1. From the realistic assumption, the potential of node B is also V_1 And hence potential of G is also V_1.

The node D potential of opamp A_2 is V_2. the potential of node C is also V_2 and hence potential of H is also V_2.

The input current of op-amp A_1 and A_2 both are zero.

Hence current I remains same through R_{f1}, R_G and R_{f2}.

Applying ohm's law btw the nodes E and F we get.

$$I = \frac{V_{01} - V_{02}}{R_{f1} + R_G + R_{f2}}$$

let $R_{f1} = R_{f2} = R_f$

$$I = \frac{V_{01} - V_{02}}{2R_f + R_G} \quad \text{---} (1)$$

From node G and H

$$I = \frac{V_G - V_H}{R_G} = \frac{V_1 - V_2}{R_G} \quad \text{---} (2)$$

Equating eqn (1) and (2) we get

$$\frac{V_{01} - V_{02}}{2R_f + R_G} = \frac{V_1 - V_2}{R_G}$$

$$\frac{V_{02} - V_{01}}{2R_f + R_G} = \frac{V_2 - V_1}{R_G}$$

$$V_{02} - V_{01} = \frac{(2R_f + R_G)(V_2 - V_1)}{R_G}$$

we know that

$$V_0 = \frac{R_2}{R_1}(V_{02} - V_{01}).$$

Substitute the value of $V_{02} - V_{01}$ in the above equation we get

$$V_0 = \frac{R_2}{R_1}\left[\frac{(2R_f + R_G)(V_2 - V_1)}{R_G}\right]$$

$$V_0 = \frac{R_2}{R_1}\left(1 + \frac{2R_f}{R_G}\right)(V_2 - V_1)$$

This is the overall gain of the circuit.

2.10.4 Instrumentation amplifier using transducer bridge

The circuit uses a resistive transducer whose resistance changes as a function of the physical quantity to be measured.

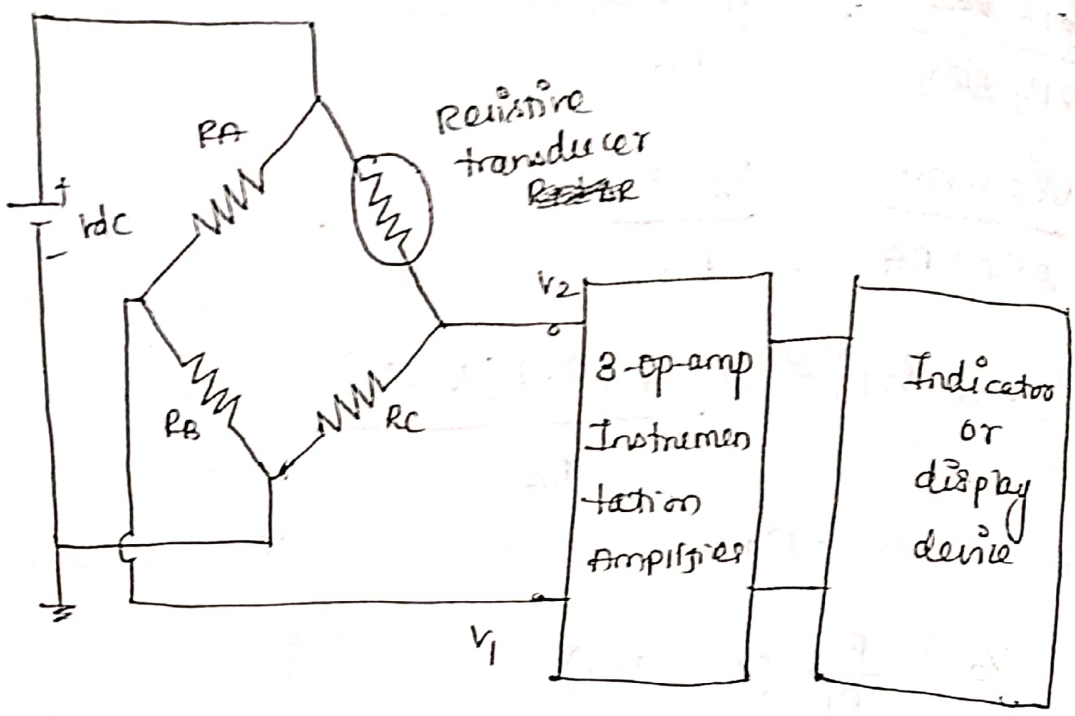


Fig 2.10.4 Instrumentation amplifier using transducer bridge

The bridge is initially balanced by a dc supply voltage Vdc so that $V_1 = V_2$. As the physical quantity changes, the resistance Rf of the transducer also changes causing an unbalance in the bridge ($V_1 \neq V_2$).

This differential voltage now gets amplified by the three op-amp differential Instrumentation amplifier. Some of the practical applications of Instrumentation amplifier are

1) Temperature indicator
2) Temperature controller
3) Light intensity meter

2.13 Log Amplifier :-

The fundamental log-amp circuit is shown in figure.

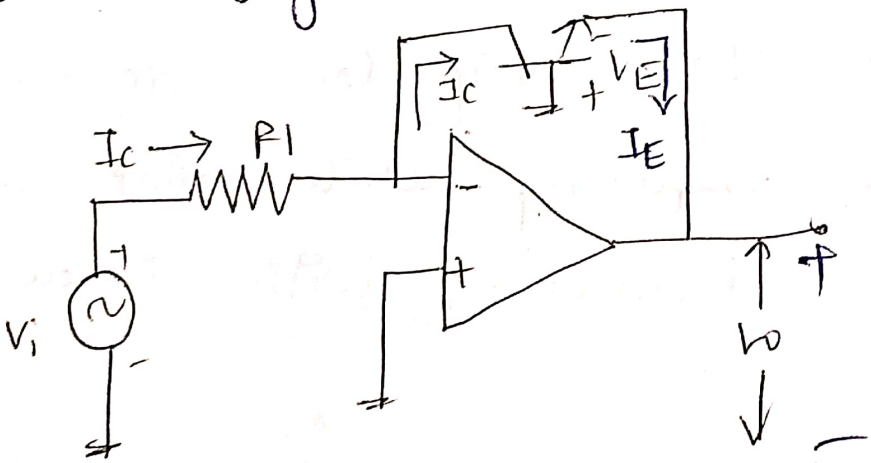


fig 2.13.1 fundamental log-amp circuit

Since the collector is held at virtual ground and the base is also grounded, the transistor's voltage - current relationship is given by

$$I_E = I_s \left(e^{qV_E/kT} - 1\right)$$

$I_E = I_C$ for a grounded base transistor.

$$\therefore \quad I_C = I_s \left(e^{qV_E/kT} - 1\right)$$

$I_s \rightarrow$ Emitter saturation current.

$k \rightarrow$ Boltzmann's constant.

$T \rightarrow$ Absolute temperature

$$\therefore \quad \frac{I_C}{I_S} = \left(e^{qV_E/kT} - 1\right)$$

$$e^{qV_E/kT} = \frac{I_C}{I_S} + 1$$

$$\approx \frac{I_C}{I_S} \qquad [\because I_C >> I_S]$$

Taking natural log on both sides, we get

$$qV_E/kT = \ln \frac{I_C}{I_S}$$

$$V_E = \frac{kT}{q} \ln\left(\frac{I_C}{I_S}\right)$$

$$I_C = \frac{V_i}{R_1}$$

Also $V_E = -V_o$

$$\therefore V_o = \frac{-kT}{q} \ln\left(\frac{V_i}{R_1 I_S}\right)$$

$$\boxed{V_o = \frac{-kT}{q} \ln \frac{V_i}{V_{ref}}}$$

$V_{ref} = R_1 I_S$

∴ The o/p voltage is proportional to the logarithm of input voltage.

Although the circuit gives natural log(ln) one can find $\log_{10}$ by proper scaling.

$$\log_{10} X = 0.4343 \ln X.$$

The circuit however has one problem. the emitter saturation current I_S varies from transistor to transistor with temperature.

Thus a stable reference voltage V_{ref} cannot be obtained. This is eliminated by log amplifies with saturation current and temperature compensation.

The input is applied to the log-amp, while a reference voltage is applied to another log amp.

The two transistors are integrated close together in the same silicon wafer. This provides a close match of saturation currents and ensures good thermal tracking.

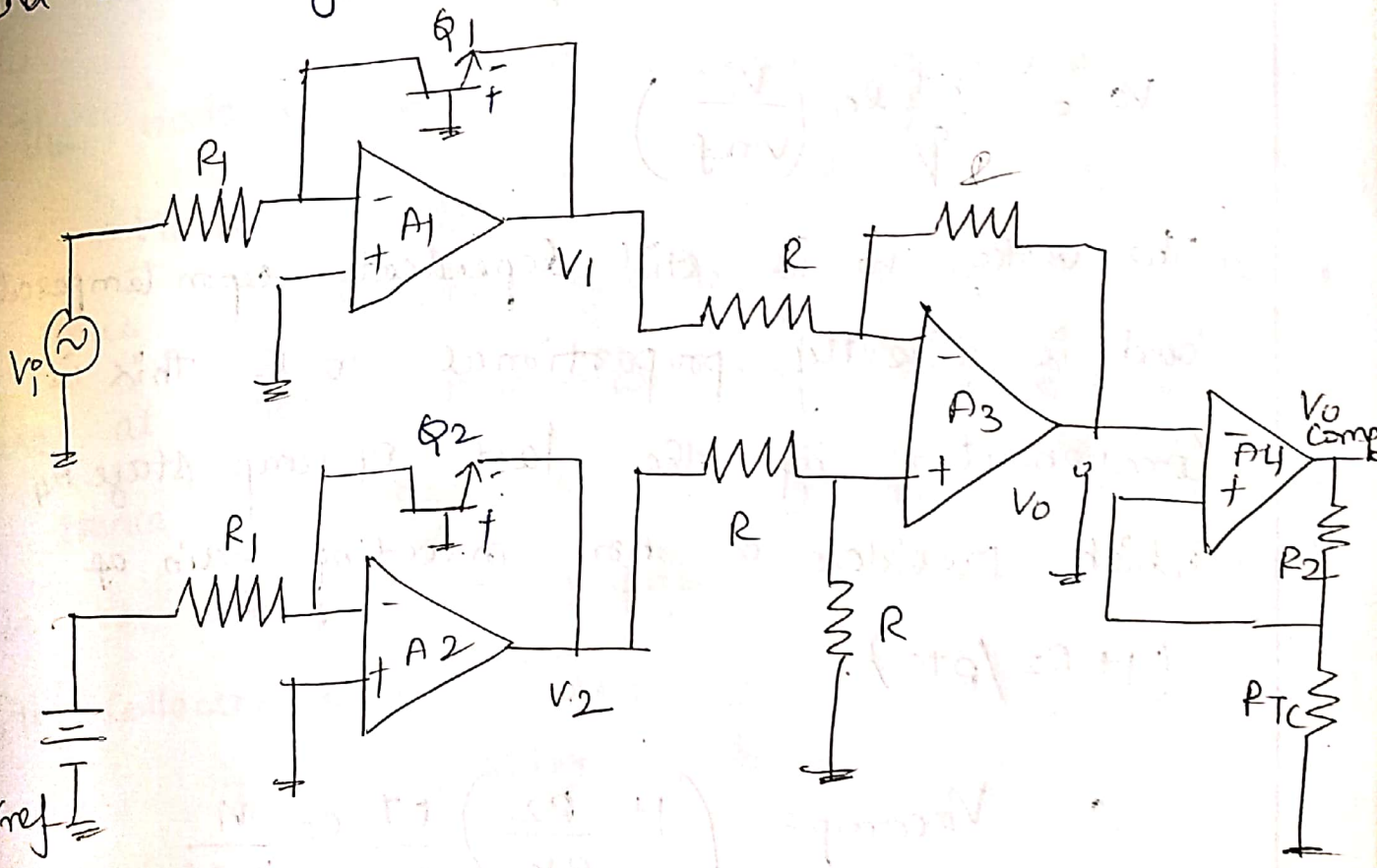


Fig 2.18.2 log amp with saturation current and temperature compensation.

Assume that $I_{S1} = I_{S2} = I_S$

Proof :

$$V_1 = -\frac{kT}{q} \ln\left(\frac{V_i}{R_1 I_S}\right)$$

$$V_2 = -\frac{KT}{q} \ln\left(\frac{V_{ref}}{R_1 I_S}\right)$$

$$V_0 = V_2 - V_1$$

$$= -\frac{KT}{q}\left[\ln \frac{V_{ref}}{R_1 I_S}\right] - \left\{-\left[\frac{KT}{q} \ln \frac{V_i}{R_1 I_S}\right]\right\}$$

$$= \frac{KT}{q} \ln \frac{V_i}{R_1 I_S} - \frac{KT}{q} \ln \frac{V_{ref}}{R_1 I_S}$$

$$V_0 = \frac{KT}{q} \ln\left(\frac{V_i}{V_{ref}}\right)$$

The voltage V_0 is still dependent upon temperature and is directly proportional to T. This is compensated by the last op amp stage A_4 which provides a non inverting gain of $(1 + R_2/R_{TC})$.

$$\therefore V_{0comp} = \left(1 + \frac{R_2}{R_{TC}}\right)\frac{KT}{q} \ln \frac{V_i}{V_{ref}}$$

where R_{TC} is a temperature sensitive resistance with a positive coefficient of temperature.

2.11 Antilog Amplifier :

2.11.1 Antilog amplifier using transistor :

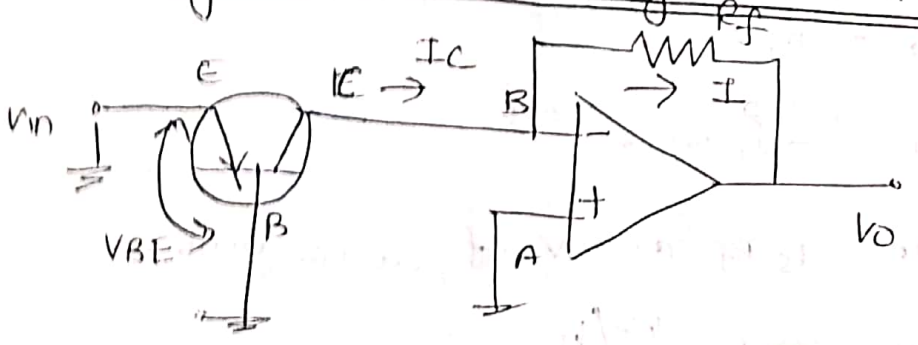


Fig 2.11.1 Basic antilog amplifier.

The node B is at virtual ground.

$\therefore V_B = 0$.

Thus both collector and base of the transistor are at ground potential and $V_{CB} = 0$

Hence the voltage across the transistor is V_{BE}, and we can write the expression for the collector current as

$$I_C = I_S e^{V_{BE}/V_T}$$

But $V_{BE} = V_{in}$

$$\therefore I_C = I_S e^{V_{in}/V_T} \quad \text{— (1)}$$

$I_C = I$ so $I = I_C = \dfrac{V_B - V_o}{R_f} = \dfrac{-V_o}{R_f}$ — (2)

equate (1) & (2)

$$\frac{-V_o}{R_f} = I_s e^{V_{in}/V_T}$$

$$\therefore V_o = R_f I_s e^{V_{in}/V_T}$$

$$V_o = -I_s R_f e^{V_{in}/V_T}$$

Assume $I_s R_f$ as V_{ref}, we can write

$$V_o = -V_{ref} e^{V_{in}/V_T}$$

Thus the output voltage is proportional to the expotential of V_{in} (or) antilog of V_{in}. Thus circuit works as basic antilog amplifier.

In the above circuits, it can be seen that the terms, I_o, I_s and V_T are present in the output equation. All these are the function of temperature.

Hence as temperature changes, these parameters also change and cause serious errors at the output. so the basic antilog circuits also face the same limitation as that of basic log amplifies circuits.

And hence temperature compensation is must for the antilog amplifier circuits as well.

14.2 Temperature Compensated Antilogarithmic Amplifier.

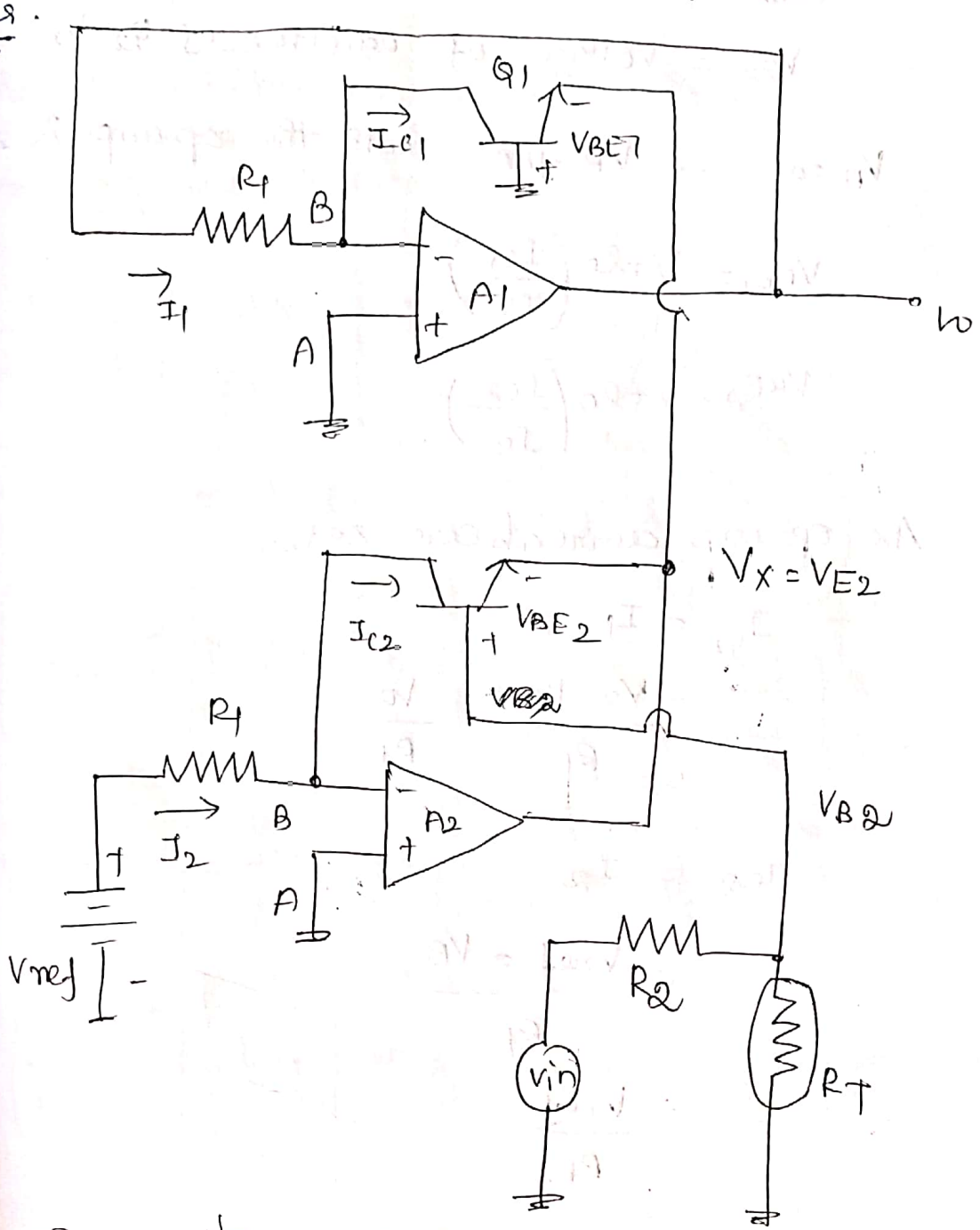


Fig 14.2 Temperature Compensated Antilog amplifier.

The two matched transistors Q_1 and Q_2 are used. The external voltage Vref is connected to inverting terminal of Op-amp A_2 through resistance R_1.

V_{B2} = voltage of base of Q2

V_{E2} = voltage of emitter of $Q_2 = V_x$

$V_A = 0$ ∴ V_B for both the op-amp is zero.

$$V_{BE_1} = V_T \ln\left(\frac{I_{C1}}{I_S}\right)$$

$$V_{BE_2} = V_T \ln\left(\frac{I_{C2}}{I_S}\right).$$

As op-amp currents are zero.

$$I_{C_1} = I_1$$

$$= \frac{V_o - V_B}{R_1} = \frac{V_o}{R_1}$$

$$I_{C2} = I_2$$

$$= \frac{V_{ref} - V_B}{R_1}$$

$$= \frac{V_{ref}}{R_1}.$$

$$V_{BE_1} = V_T \ln\left(\frac{V_o}{R_1 I_S}\right)$$

$$V_{BE_2} = V_T \ln\left(\frac{V_{ref}}{I_S R_1}\right)$$

The voltage $V_x = -V_{BE_1} = -V_T \ln\left(\frac{V_o}{R_1 I_S}\right)$

$$V_{B2} = \frac{V_{in} R_T}{R_2 + R_T}.$$

for the transistor Q2, we can write.

$$V_{B2} = V_{E2} + V_{BE2}$$

$$V_{in}\left[\frac{R_T}{R_2+R_T}\right] = V_X + V_T \ln\left(\frac{V_{ref}}{I_S R_1}\right)$$

$$= -V_T \ln\left(\frac{V_o}{I_S R_1}\right) + V_T \ln\left(\frac{V_{ref}}{I_S R_1}\right)$$

$$V_{in}\left[\frac{R_T}{R_2+R_T}\right] = -V_T\left[\ln\left(\frac{V_o}{R_1 I_S}\right) - \ln\left(\frac{V_{ref}}{I_S R_1}\right)\right]$$

$$V_{in}\left[\frac{R_T}{R_2+R_T}\right] = -V_T\left[\ln\left(\frac{V_o}{R_1}\right) - \ln(I_S) - \ln\left(\frac{V_{ref}}{R_1}\right) + \ln(I_S)\right]$$

$$\frac{V_{in}}{V_T}\left[\frac{R_T}{R_2+R_T}\right] = -\left[\ln\left(\frac{V_o}{R_1}\right) - \ln(I_S) - \ln\left(\frac{V_{ref}}{R_1}\right) + \ln(I_S)\right]$$

$$= \ln\left(\frac{V_{ref}}{R_1}\right) - \ln\left(\frac{V_o}{R_1}\right)$$

$$= \ln\left[\frac{V_{ref} - V_o}{R_1}\right]$$

$$\frac{V_{in}}{V_T}\left[\frac{R_T}{R_2+R_T}\right] = -\ln\left[\frac{V_o}{V_{ref}}\right]$$

$$\ln\left(\frac{V_0}{V_{ref}}\right) = -\frac{V_{in}}{V_T}\left[\frac{R_T}{R_2+R_T}\right]$$

$$\frac{V_0}{V_{ref}} = \ln^{-1}\left[\frac{-V_{in}R_T}{V_T(R_2+R_T)}\right]$$

$$V_0 = V_{ref}\ln^{-1}\left[\frac{-V_{in}R_T}{V_T(R_2+R_T)}\right]$$

Thus the output is proportional to the antilog ($\ln^{-1}$) of the input. The term $\frac{R_T}{V_T(R_2+R_T)}$ is constant through temperature changes as R_T also changes proportional to the changes in V_T.

Thus a complete temperature compensation is achieved with this circuit.

2.11 Integrator :-

In an integrator circuit, the output voltage is the integration of the input voltage. The integrator circuit can be obtained without using active devices like op-amp, transistors etc. In such a case an integrator is called passive Integrator.

while an Integrator using an active devices like op-amp is called active Integrator.

2.11.1 Ideal Active op-amp Integrator :-

Consider the op-amp integrator circuit as shown in figure.

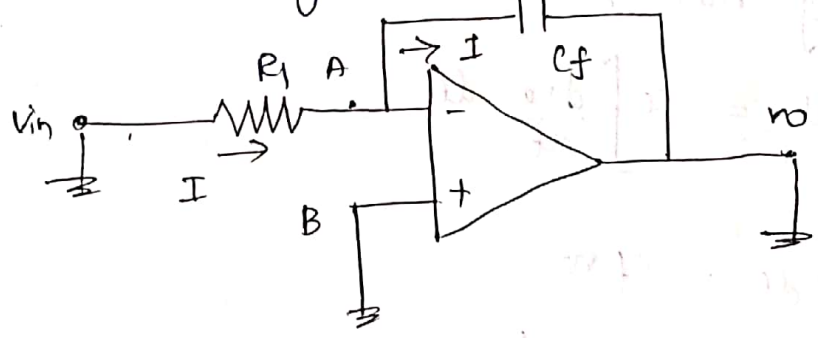


Fig 2.11.1 op-amp Integrator

The node B is grounded. The node A is also at the ground potential from the concept of virtual ground.

$$V_A = 0 = V_B .$$

The current I flows through the resistor R_1 & capacitor Cf.

From the input side we can write

$$I = \frac{V_{in} - V_A}{R_1} \qquad V_A = 0$$

$$I = \frac{V_{in}}{R_1} \quad \text{—①}$$

From the output side we can write

$$I = \frac{C_f \, d(V_A - V_o)}{dt} \qquad V_A = 0$$

$$I = -C_f \frac{dv_o}{dt} \quad \text{—②}$$

Equating eqn ① & ②

$$\frac{V_{in}}{R_1} = -C_f \frac{dv_o}{dt}$$

Integrating both sides

$$\int_0^t \frac{v_{in}}{R_1} dt = -C_f \int \frac{dv_o}{dt} dt$$

$$\int_0^t \frac{v_{in}}{R_1} dt = -C_f v_o$$

$$\therefore \boxed{V_o = -\frac{1}{R_1 C_f} \int_0^t V_{in} dt + V_o(0)} \quad \text{—③}$$

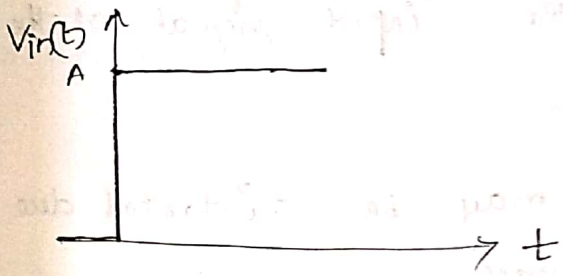
where $V_o(0)$ is the constant of Integration indicating the initial output voltage.

From the above equation, the output is $\frac{-1}{R_1 C_f}$ times the integral of input and $R_1 C_f$ is called time constant of the integrator.

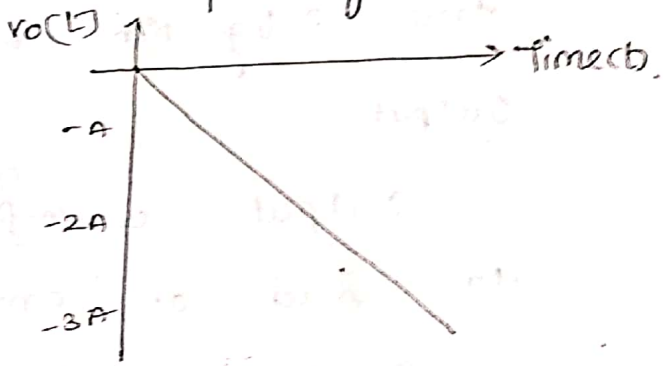
The negative sign indicates that there is a phase shift of 180° between input and output.

2.11.2 Input and output waveforms :-

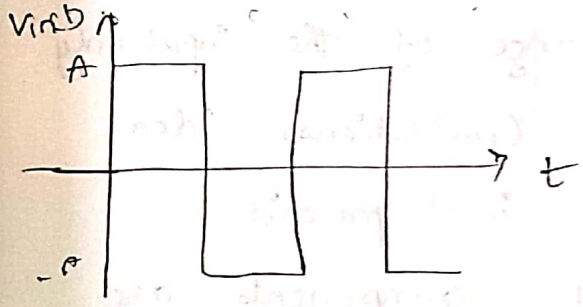
i) Step input signal.



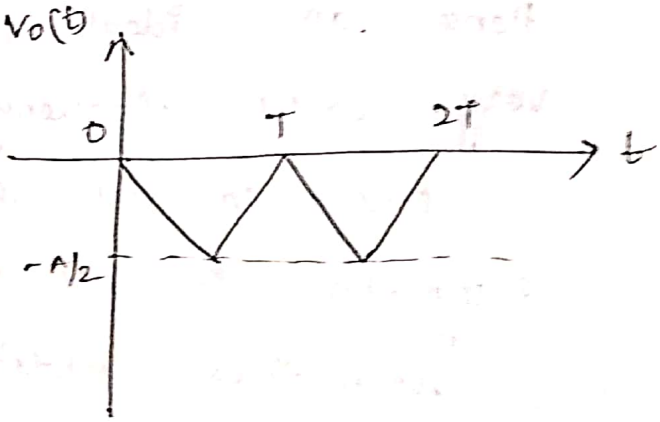
output signal.



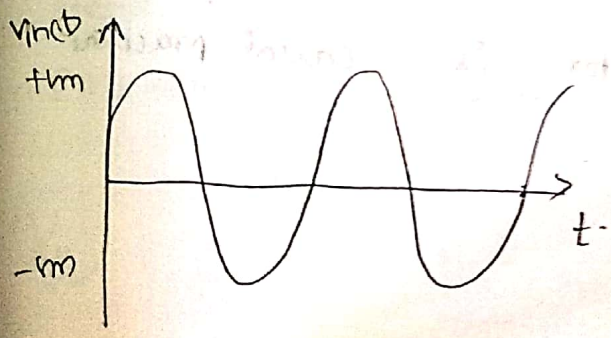
ii) square wave input signal.



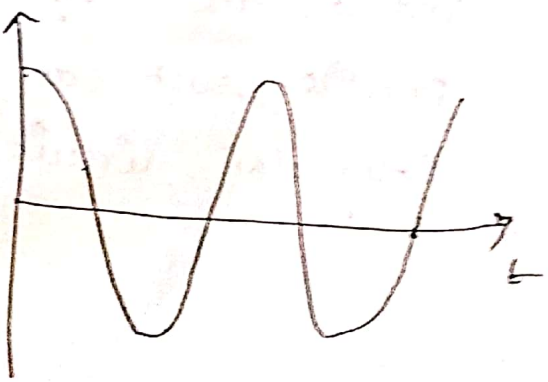
output signal.



iii) sine wave input signal.



Vo(t)



2.11.3 Errors in an Ideal Integrator:

In the presence of the input signal, the two components namely offset voltage and bias current, contribute an error voltage at the output. Thus it is not possible to get a true integration of the input signal at the output.

Output waveform may be distorted due to such an error voltage.

Another limitation of an ideal integrator is its bandwidth, which is very small. Hence an ideal integrator can be used for a very small frequency range of the input only.

Due to all these limitations, ideal integrator is not used in practice.

Sometimes additional components are used along with basic integrator circuit to reduce the effect of an error voltage in practice. Such an integrator is called practical integrator circuit.

2.11.4 Practical Integrator:-

The limitations of an ideal integrator can be minimized in the practical Integrator circuit, which uses a resistance R_f in parallel with the capacitor C_f.

The practical integrator circuit is shown in figure.

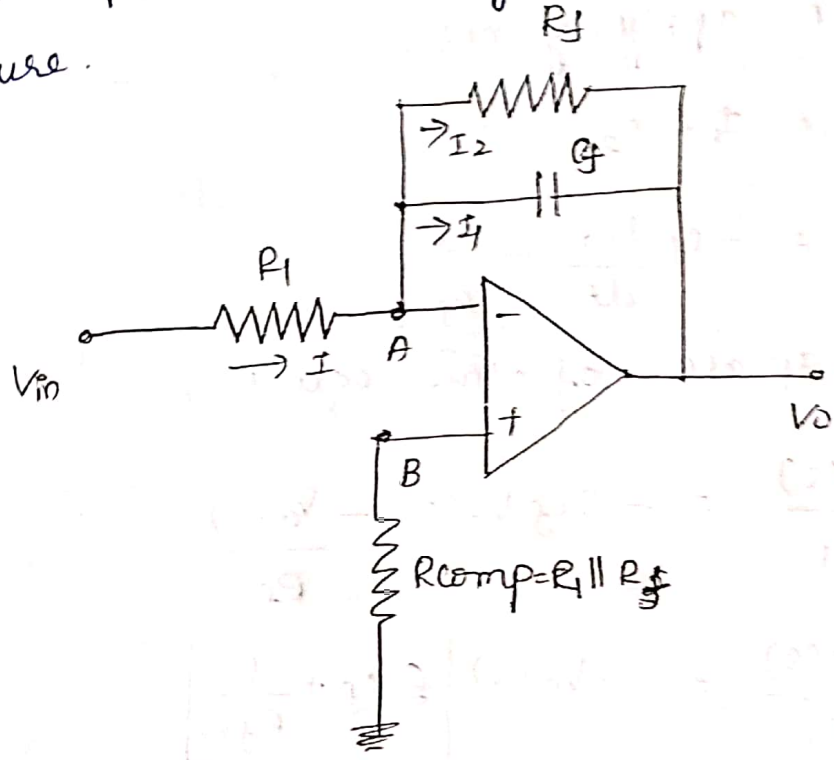


Fig 2.11.2 Practical Integrator circuit

As the input current of op amp is zero, the node B is still at ground potential. Hence the node A is also at the ground potential from the concept of virtual ground

$\therefore V_A = 0$

$$I = \frac{V_{in} - V_A}{R_1} = \frac{V_{in}}{R_1}.$$

$$I_1 = \frac{C_f \, d(V_{in} - V_o)}{dt} \qquad \because V_D = 0$$

$$= -C_f \frac{dV_o}{dt}$$

$$I_2 = \frac{V_{in} - V_o}{R_f} = \frac{-V_o}{R_f}$$

At node n, applying KCL.

$$I = I_1 + I_2$$

$$\frac{V_{in}}{R_1} = -C_f \frac{dv_o}{dt} - \frac{v_o}{R_f}$$

Take Laplace of this equation

$$\frac{V_{in}(s)}{R_1} = -sC_f V_o(s) - \frac{V_o(s)}{R_f}$$

$$\frac{V_{in}(s)}{R_1} = -V_o(s)\left[sC_f + \frac{1}{R_f}\right]$$

$$\frac{V_{in}(s)}{R_1} = -V_o(s)\left[\frac{1 + sC_f R_f}{R_f}\right]$$

$$V_o(s) = -\left[\frac{\frac{V_{in}(s)}{R_1}}{\frac{1 + sC_f R_f}{R_f}}\right]$$

$$= -\frac{1}{\left(\frac{1 + sC_f R_f}{R_f}\right) R_1} V_{in}(s)$$

$$= -\frac{1}{\left(\frac{R_1}{R_f} + sC_f R_1\right)} V_{in}(s)$$

$$V_o(s) = -\frac{1}{\left(sC_f R_1 + \frac{R_1}{R_f}\right)} V_{in}(s)$$

when R_f is very large then R_1/R_f can be neglected and hence circuit behaves like an ideal integrator.

$$V_o(s) = -\frac{1}{sR_1C_f} V_{in}(s)$$

$$\boxed{V_o(t) = \frac{-1}{R_1C_f}\int V_{in}(t)\,dt.}$$

$$\frac{1}{s} = \int dt.$$

Thus the output voltage v_o is the integration of Input voltage v_{in}.

2.12. Differentiator :-

The circuit which produces the differentiation of the input voltage at its output is called differentiator.

2.12.1 Ideal Active op-amp Differentiator :-

The active integrator circuit can be obtained by exchanging the positions of R and C in

The basic active Integrator circuit

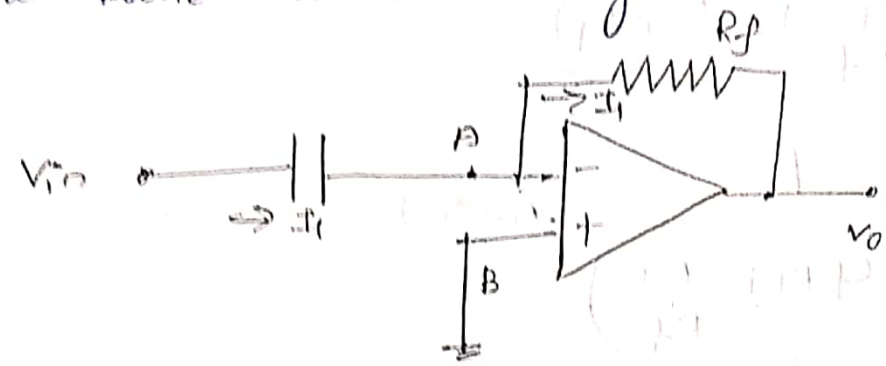


Fig 2.12.1 Op-amp differentiator.

The node B is grounded. The node A is also at the ground potential hence $V_A = 0$.

From the input side we can write

$$I_1 = C_1 \frac{d(V_{in} - V_A)}{dt} = C_1 \frac{dV_{in}}{dt} \quad -(1) \quad [\because V_A = 0]$$

From the output side we can write

$$I = \frac{V_A - V_o}{R_f} = \frac{-V_o}{R_f} \quad -(2)$$

Equating (1) & (2)

$$C_1 \frac{dV_{in}}{dt} = \frac{-V_o}{R_f}$$

$$V_o = -C_1 R_f \frac{dV_{in}}{dt}$$

The equation shows that the output is $C_1 R_f$ times the differentiation of the input and product $C_1 R_f$ is called time Constant of the differentiator.

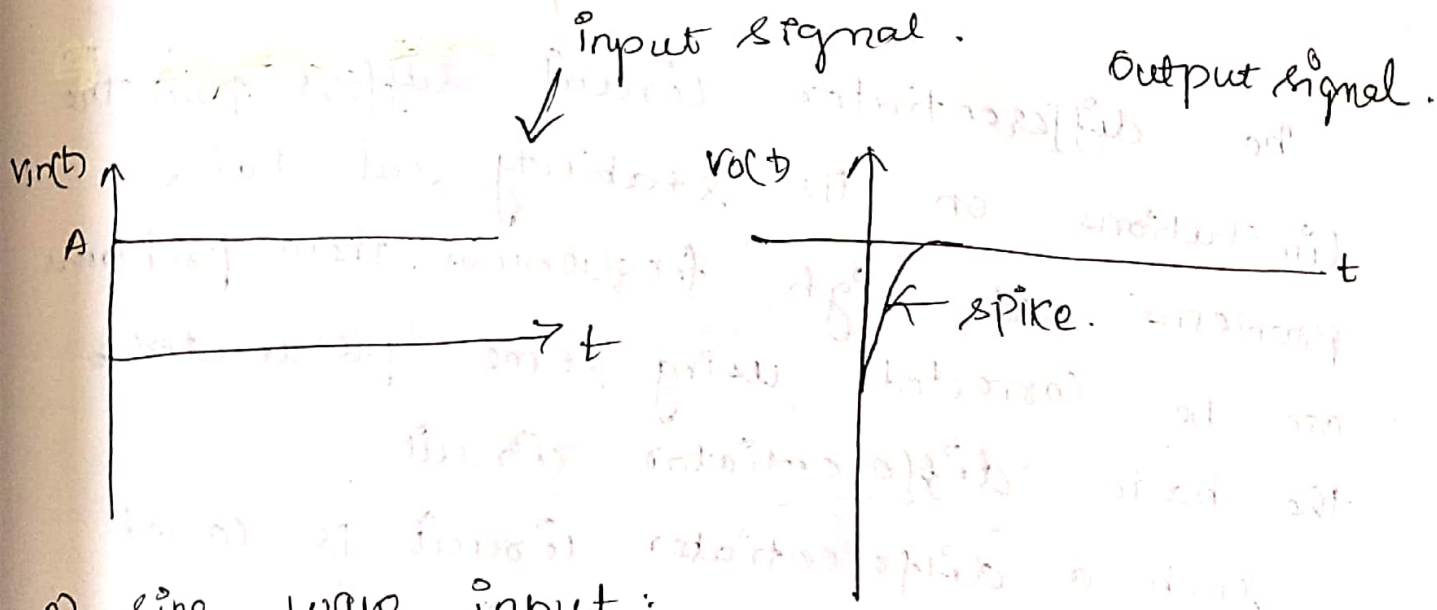
The negative sign indicates that there is a phase shift of 180° between input and output.

2.12.2 Input and output waveforms :-

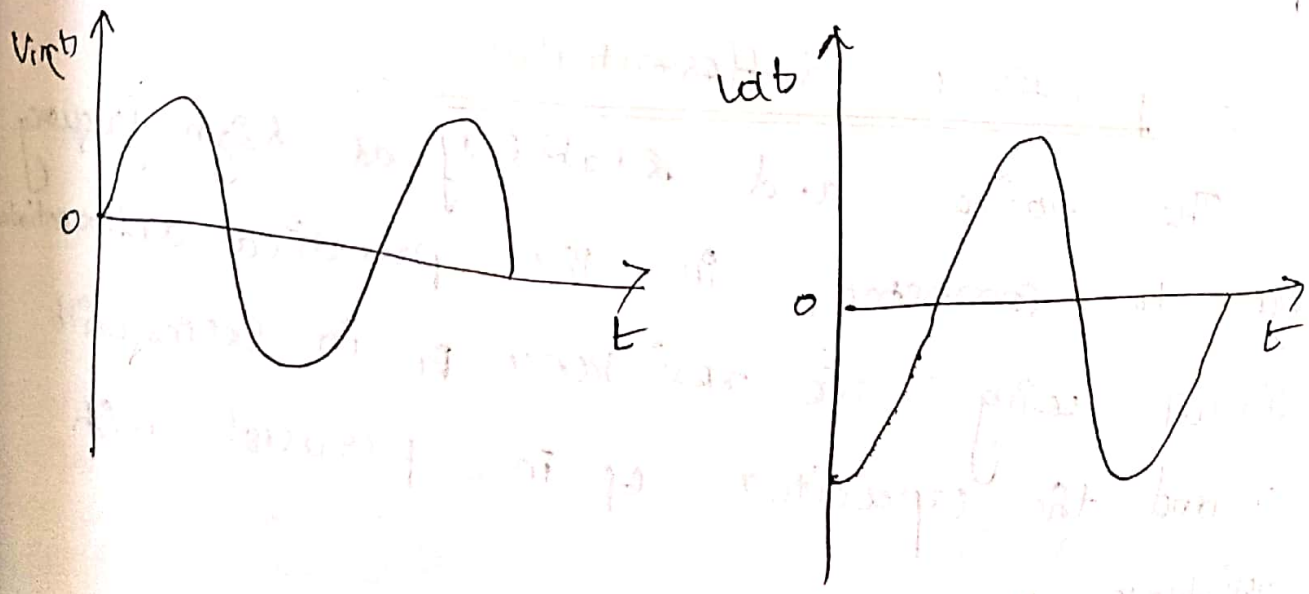
1) Step input signal.

$V_{in}(t) = A$ for $t \geq 0$

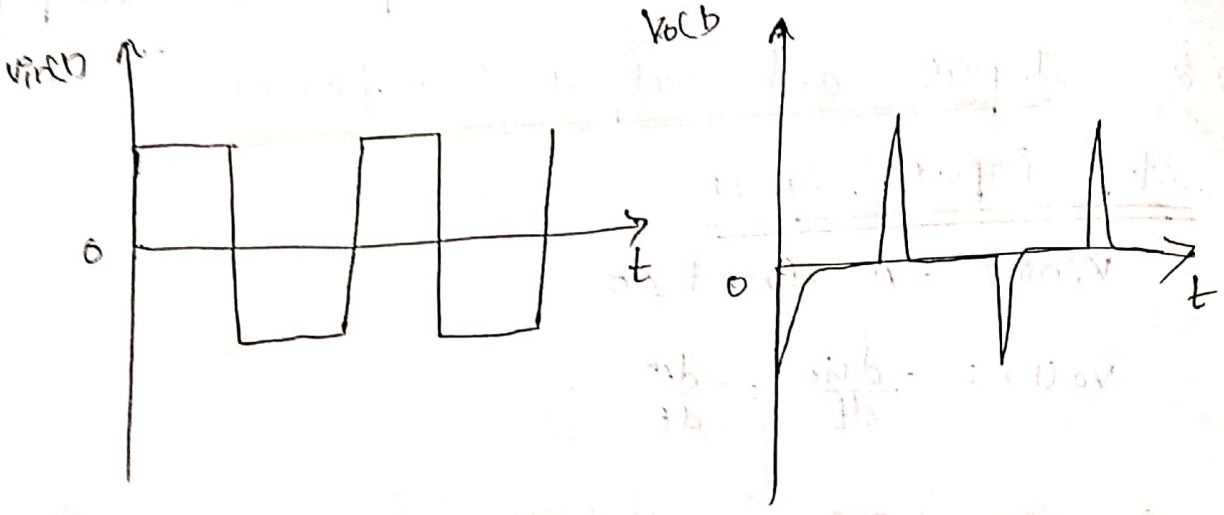
$V_o(t) = -\frac{dV_{in}}{dt} = -\frac{dA}{dt} = 0$



2) Sine wave input :



3) Square wave input signal



The differentiator circuit suffers from the limitations on its stability and noise problems at high frequencies. These problems can be corrected using some parameters in the basic differentiator circuit.

such a differentiator circuit is called practical differentiator circuit.

2.12.2 practical differentiator :

The noise and stability at high frequency can be corrected, in the practical differentiator circuit using the resistance R_1 in series with C_1 and the capacitor C_f in parallel with resistance R_f.

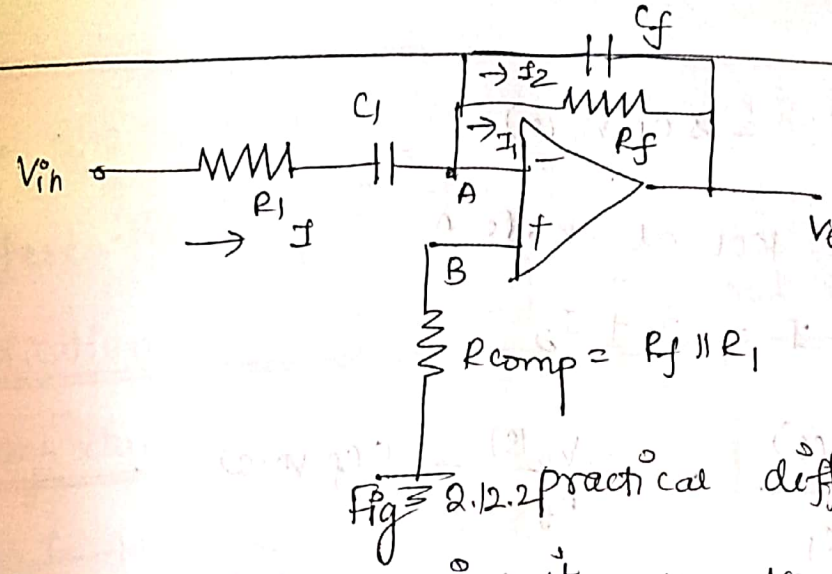


Fig 2.12.2 practical differentiator circuit

From the above circuit $V_A = V_B = 0V$.

for the current I, we can write

$$I = \frac{V_{in} - V_A}{Z_1} = \frac{V_{in}}{Z} \qquad \because V_A = 0.$$

$Z_1 = R_1$ in series with C_1.

So in laplace transform we can write.

$$Z_1 = R_1 + \frac{1}{sC_1} = \frac{1+R_1sC_1}{sC_1}$$

$$I = \frac{V_{in}(s)}{\left(\frac{1+R_1sC_1}{sC_1}\right)} = \frac{sC_1 V_{in}(s)}{1+sR_1C_1}$$

now the current I_1 is

$$I_1 = \frac{V_A - V_o}{R_f} = \frac{-V_o}{R_f}$$

In laplace $I_1 = -\frac{V_o(s)}{R_f}$

$$I_2 = C_f \frac{d(V_A - V_o)}{dt} = -C_f \frac{dV_o}{dt}$$

$$I_2 = -sC_f V_o(s).$$

Applying KCL at node A

$$I = I_1 + I_2$$

$$\frac{sC_1 V_{in}(s)}{1+sR_1C_1} = \frac{-V_o(s)}{R_f} - sC_f V_o(s)$$

$$= -V_o(s)\left[\frac{1+sC_fR_f}{R_f}\right]$$

$$V_o(s) = \frac{sC_1 V_{in}(s)}{1+sR_1C_1} \Bigg/ \frac{1+sC_fR_f}{R_f}$$

$$= \frac{-sR_fC_1 V_{in}(s)}{(1+sR_fC_f)(1+sR_1C_1)}$$

If $R_fC_f = R_1C_1$ then $\left[\because R_fC_f = R_1C_1\right]$

$$v_o(s) = \frac{-sR_fC_1 V_{in}(s)}{(1+sR_1C_1)^2}$$

The time constant R_1C_1 is much less when compared to R_fC_f.

$$\therefore V_o(s) = -sR_fC_1 V_{in}(s)$$

$$V_o(t) = -R_fC_1 \frac{d\,v_{in}(t)}{dt} \quad \because s = \frac{d}{dt}$$

Thus the output voltage is the $R_f C_1$ times the differentiation of the input.

2.12.4 Applications of practical Integrator & Differentiator.

Integrator

1) In the analog computers
2) Analog to digital compu convertor
3) Ramp generators
4) Various signal wave shaping circuits.

Differentiator.

1) FM demodulators.
2) In the wave shaping circuits to detect the high frequency components in the input signal.

2.12.5 Why integrators are preferred in Analog Computers?

The gain of the integrator decreases with increase in the frequency while that of the differentiator increases with increase in the frequency.

Hence it is very easy to stabilise the integrator with respect to the spurious oscillations

The integrator is less sensitive to noise voltages.

The input impedance of the integrator is constant, not a function of frequency while the input impedance of the differentiator decreases as the frequency increases.

Overall the integrator is more stable than the differentiator and less sensitive to noise and hence chances of oscillations are much less in the integrator.

Due to all these reasons the integrator are preferred in the analog computers.

2.15 Comparators:-

A Comparator is a circuit which compares a signal voltage applied at one input of an op-amp with a known reference voltage at the other input and produce either

a high or low output voltage, depending on which input is higher.

It produces output voltage which is either positive saturation voltage (+Vsat) or negative saturation voltage (-Vsat).

As comparator output has two voltage levels, either high or low it is not linearly proportional to input voltage.

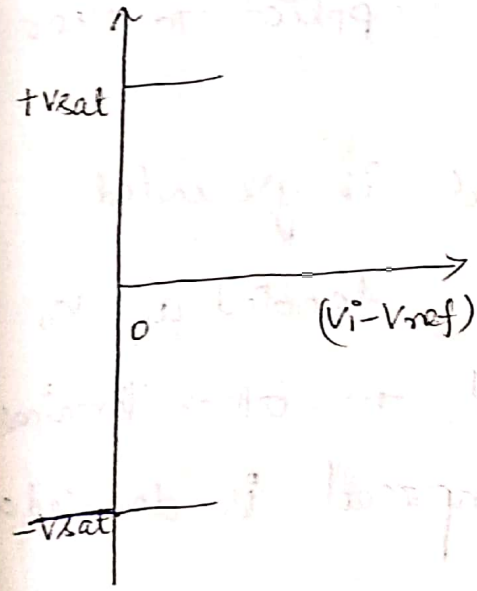


Fig 2.15.1 Transfer characteristics of Ideal comparator

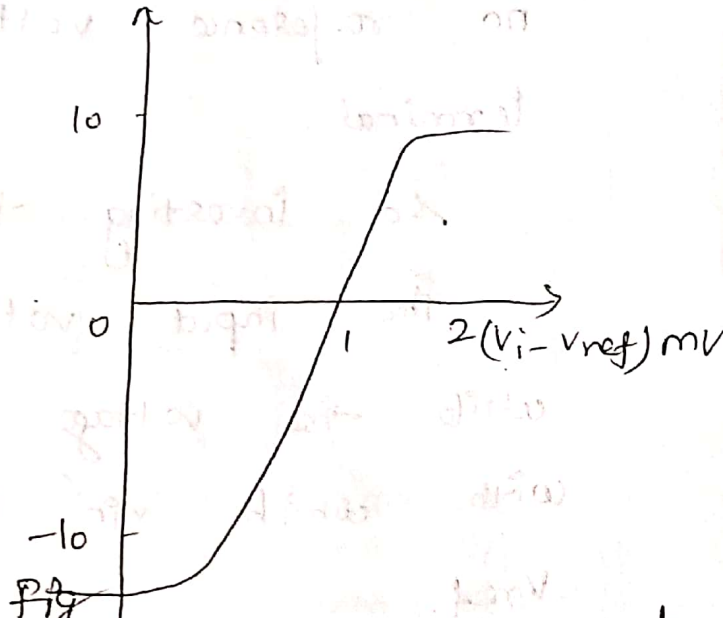


Fig 2.15.2 practical comparator

The op-amp is used in a open loop configuration for a comparator.

There are two types of comparator circuits

1. non-inverting comparator 2. Inverting comparator

2.15.1 Basic non-inverting comparator:-

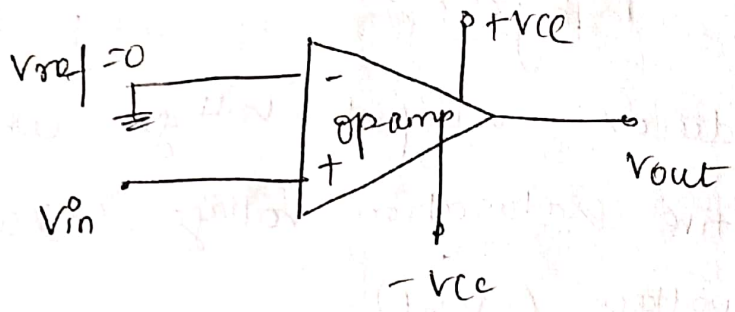


Fig 2.15.2 Basic non inverting comparator

In this comparator, the input voltage is applied to the non inverting terminal and no reference voltage is applied to other terminal.

So inverting terminal is grounded.

The input voltage is denoted as V_{in} while the voltage applied to other terminal with which V_{in} is compared is denoted as V_{ref}.

In the basic comparator $V_{ref} = 0$.

If $V_{in} > V_{ref}$ then output is $+V_{sat}$ (i) almost equal to $+V_{CC}$.

If $V_{in} < V_{ref}$ then output is $-V_{sat}$ (ii) almost equal to $-V_{EE}$.

$V_{ref} = 0V$ when v_{in} is positive then $v_o = +V_{sat}$, when v_{in} is negative then $v_o = -V_{sat}$

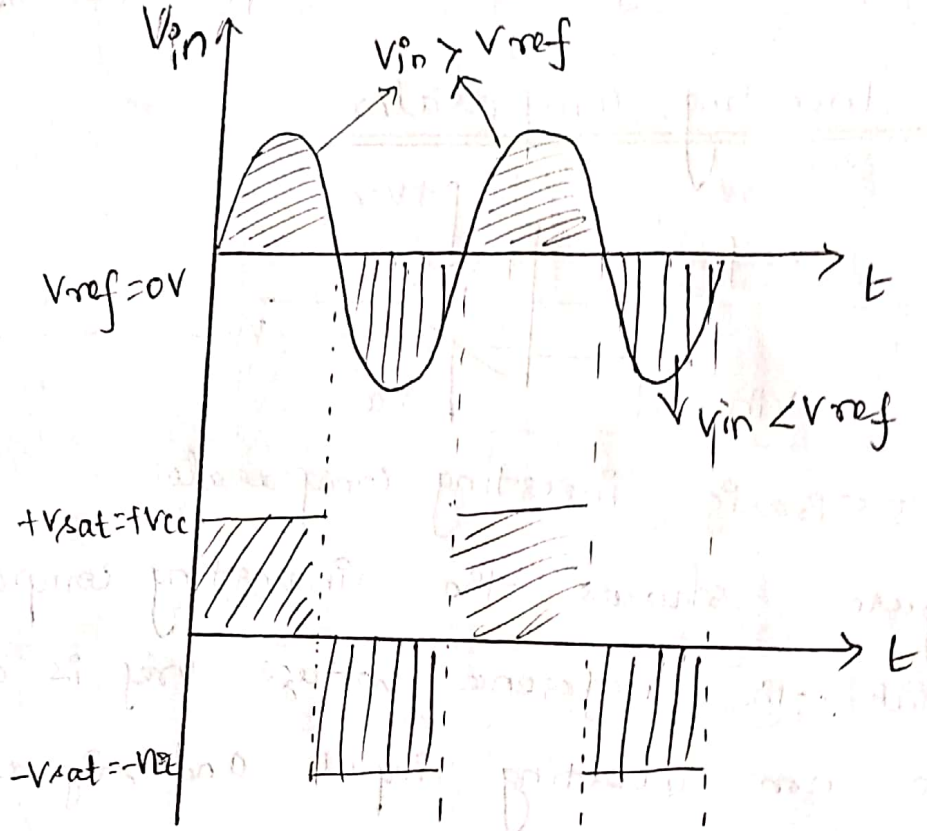
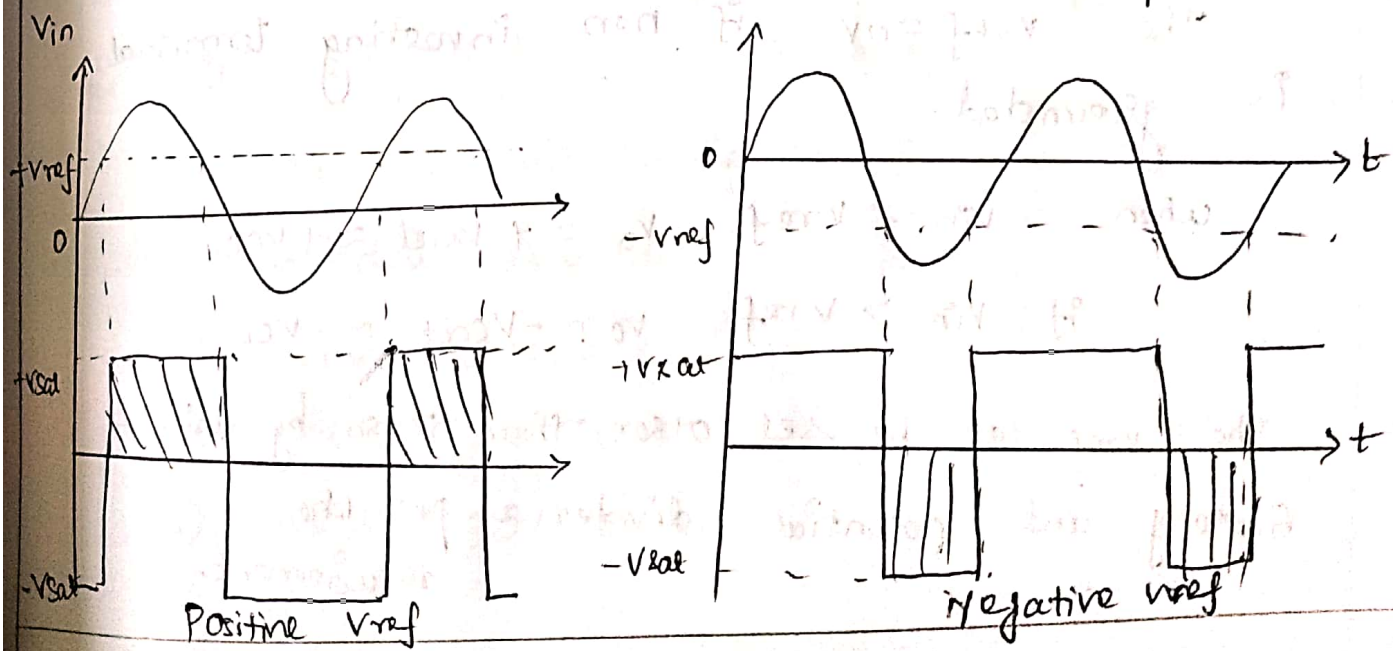


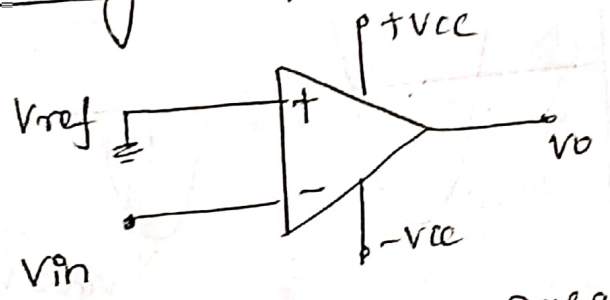
Fig 2.15.4 waveforms of a basic non inverting comparator.



Vin is compared with the reference voltage Vref applied to the inverting terminal.

If Vin > Vref then the output is +Vsat while if Vin < Vref then the output is -Vsat.

2.15.2 Basic Inverting comparator



2.15.5 Basic inverting comparator

Figure shows the inverting comparator in which the reference voltage Vref is applied to the non-inverting input and signal voltage Vin is applied to the inverting input of the op-amp.

The Vref = 0V if non inverting terminal is grounded.

when Vin < Vref $V_o = +V_{sat} \simeq +V_{CC}$

if Vin > Vref $V_o = -V_{sat} \simeq -V_{EE}$

The Vref can be set other than zero by using a battery and potential divider as per the requirement.

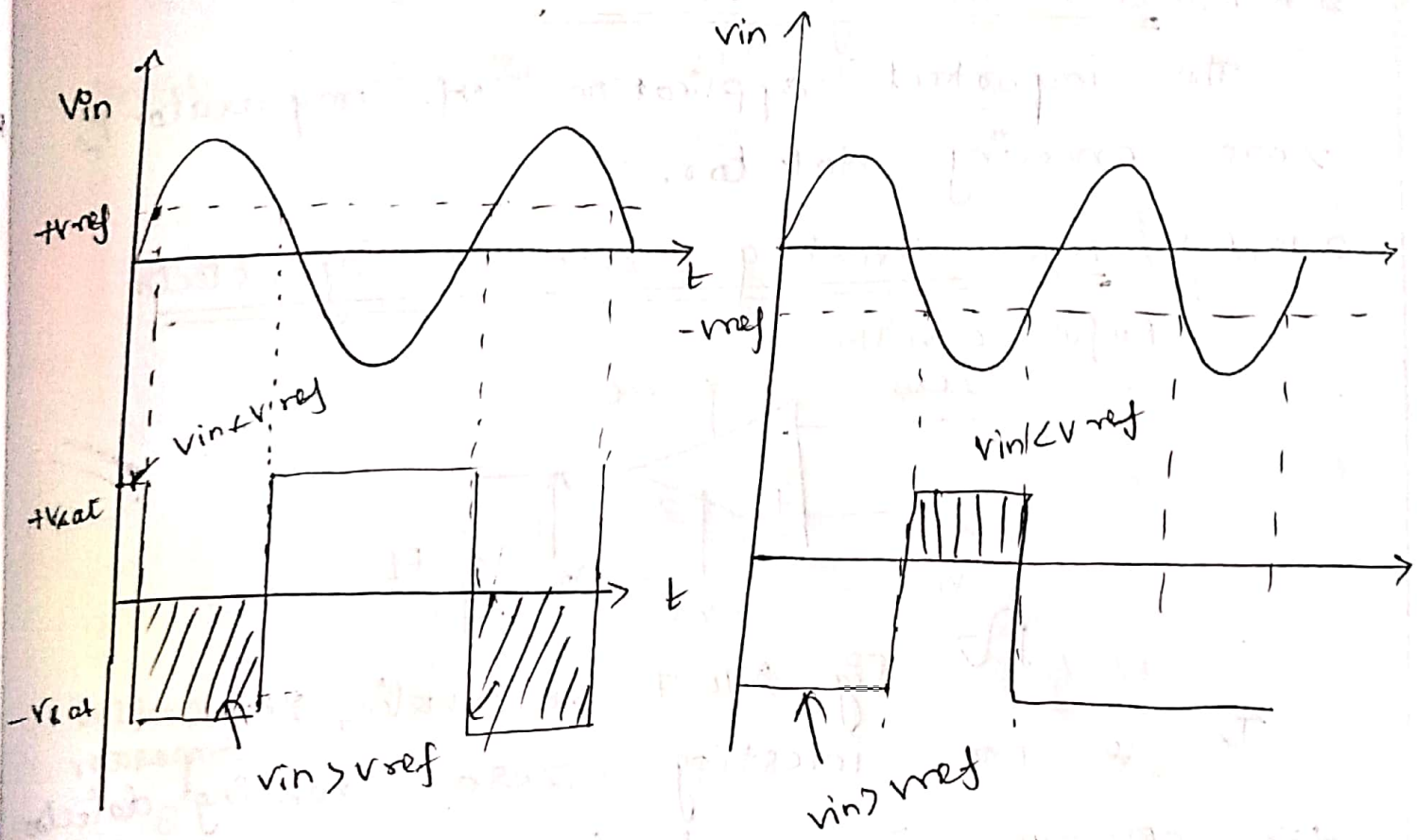


Fig 2.15.6 Input and output waveforms for Inverting comparator.

2.15.3. Applications.

The various applications of comparator circuit are

1) zero crossing detectors
2) window detector
3) Level detector
4) Duty cycle controller
5) pulse generator.

2.16 Schmitt Trigger (Regenerative Comparator)

In a basic comparator, a feedback is not used and the op-amp is used in the open loop mode.

As open loop gain of op-amp is large, very small noise voltages also can cause triggering of the Comparator, to change its state.

Such a false triggering may cause lot of problems in the applications of Comparator as zero crossing detector.

The comparator circuits used to avoid such unwanted triggering is called regenerative Comparator or schmitt trigger, which basically uses a positive feedback.

Figure shows such a regenerative Comparator. The input voltage is applied to the inverting terminal and feedback voltage to the non inverting terminal.

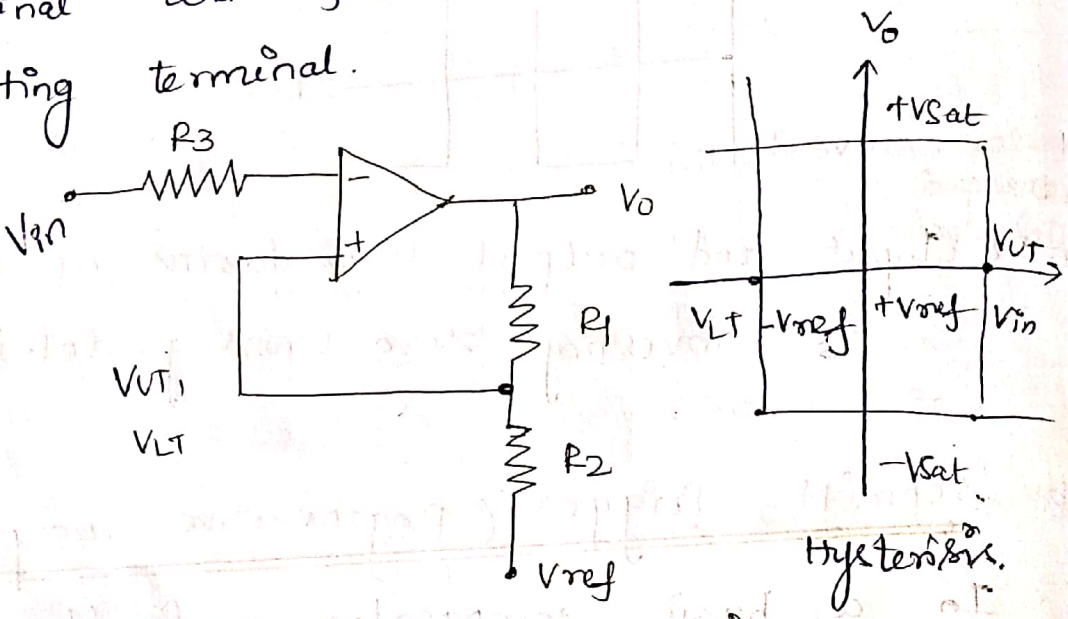


Fig 2.16.1 An inverting schmitt trigger.

The input voltage V_i triggers the output V_o everytime it exceeds certain voltage levels. These voltage levels are called upper threshold voltage (V_{UT}) and lower threshold voltage (V_{LT}).

The hysterisis width is the difference between these two threshold voltages.

(ii) $V_{UT} - V_{LT}$.

Suppose the output $V_o = +V_{sat}$. The voltage at non inverting input terminal can be obtained by using superposition

$$V_{UT} = \frac{V_{ref} R_1}{R_1 + R_2} + \frac{R_2 V_{sat}}{R_1 + R_2}$$

This voltage is called upper threshold voltage V_{UT}. As long as V_i is less than V_{UT}, the O/P V_o remains constant at $+V_{sat}$.

when V_i is just greater than V_{UT}, the output regeneratively switches to $-V_{sat}$ and remains at this level as long as $V_i > V_{UT}$.

for $V_o = -V_{sat}$, the voltage at non inverting input terminal is

$$V_{LT} = \frac{V_{ref} R_1}{R_1 + R_2} - \frac{R_2 V_{sat}}{R_1 + R_2}$$

$V_i > V_{UT} = +V_{sat}$

$V_i < V_{UT} = +V_{sat}$

This voltage is referred to as lower threshold voltage V_{LT}. The input voltage V_i must become lesser than V_{LT} in order to cause V_o to switch from $-V_{sat}$ to $+V_{sat}$.

Note that $V_{LT} < V_{UT}$ and the difference between these two voltages is the hysteresis

width V_H and can be written as

$$V_H = V_{UT} - V_{LT} = \frac{2R_2 V_{sat}}{R_1 + R_2}.$$

$V_i < V_{UT} = +V_{sat}$

$V_i > V_{UT} = -V_{sat}$

$V_i < V_{LT} = +V_{sat}$

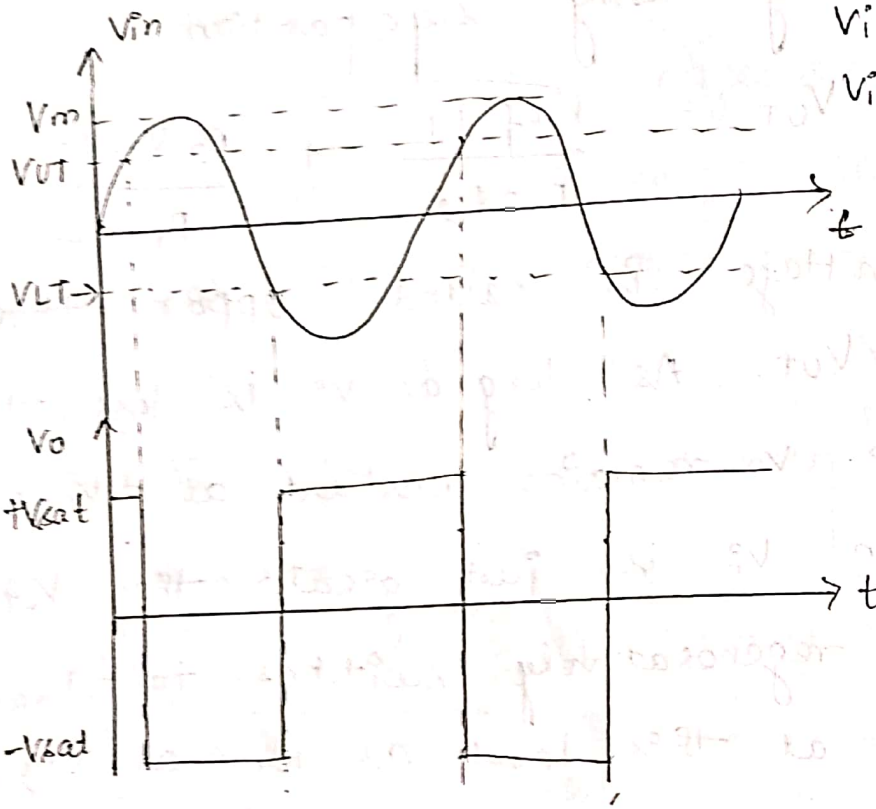


Fig 2.16 Input and output waveforms of Inverting schmitt trigger.

2.16.1. Comparison of schmitt Trigger and Comparator.

schmitt Trigger	Comparator
1. Feedback is used	Feedback is not used.
2. The op-amp is used is in closed loop mode.	opamp is used is in open loop mode.

Schmitt trigger	Comparator
3. The two different threshold voltages exist as V_{UT} and V_{LT}.	A single reference voltage exists which acts as triggering voltage (ie) V_{ref} or $-V_{ref}$.
4. Hysteresis exists with a width $H = V_{UT} - V_{LT}$	Hysteresis does not exists.
5. The various applications are 1) square wave generators. 2) ON-OFF controllers 3) To convert any waveform to square wave	5. 1) zero crossing detector 2) window detector 3) Level detector 4) Pulse generator.

2.7 Precision Rectifiers:

The major limitation of ordinary diode is that it cannot rectify voltages below V_γ (0.7V) the cut in voltage of the diode.

A circuit that acts like an ideal diode can be designed by placing a diode in the feedback loop of an op-amp.

The rectifiers which are used to precisely rectify voltages having amplitudes less than 0.7 Hence these circuits are called small signal precision rectifiers.

2.17.1 Precision half wave rectifier

The precision half wave rectifiers are classified as

1. positive half wave rectifier
2. negative half wave rectifier.

2.17.1.1 positive half wave rectifier:

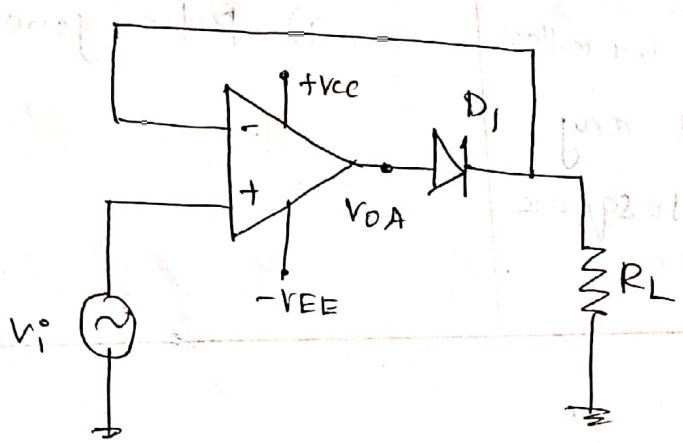


Fig 2.17.1 positive precision half wave rectifier.

The diode D is used in the feedback loop of the circuit.

When $V_i > 0$, Consider that input voltage is positive going.

Due to high open loop gain of op-amp it produces high voltage V_{on}. It makes the diode D_1 forward biased.

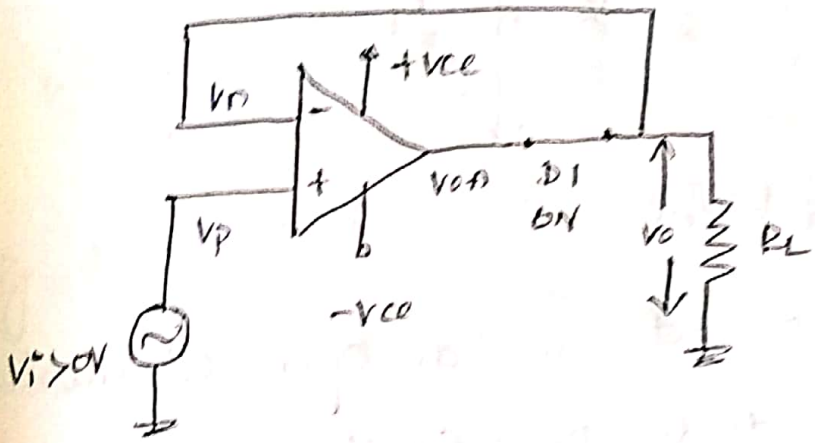


Fig 2.17.2 $V_i > 0V$.

So it acts as a ideal diode and in forward biased condition behaves as a switch. The cut in voltage of diode of 0.7V gets divided by A_{OL} which is very high. $(0.7/A_{OL})$ Hence immediately when v_i starts increasing, D_1 becomes on. Then circuit works as a voltage follower.

From virtual ground $V_n = V_p = v_i$ and $v_o = v_i$ due to feedback path - Hence entire positive half cycle is available across the load.

When v_i goes negative, immediately v_{of} produced attains that value making diode D_1 reverse biased.

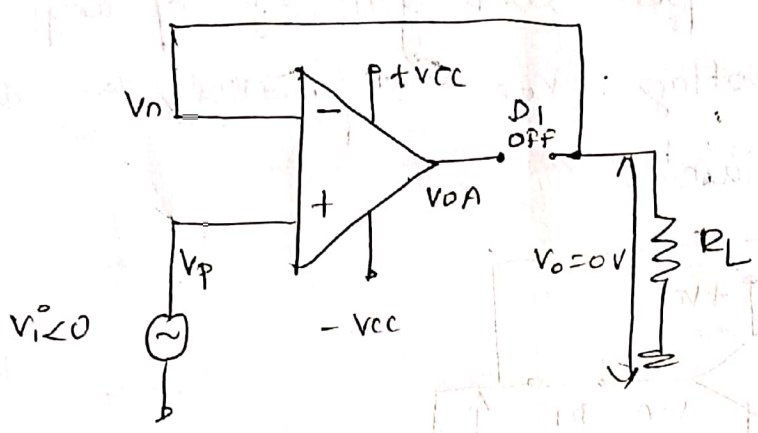


Fig 2.17(a) $V_i < 0V$

Thus diode D_1 acts as an open circuit. Due to OFF diode D_1, feedback path gets opened and no current can flow through R_L. The voltage V_o is 0V and negative half cycle of V_i gets clipped from the output. Thus compared to conventional rectifiers, precision rectifiers can rectify small voltages of the order of few millivolts.

2.A.1.2 Negative half wave rectifier

By changing the direction of D_1 in positive half wave rectifier circuit, the negative half wave rectifier can be obtained.

When V_i go (to) positive going, immediately V_{oA} is very high due to high open loop gain

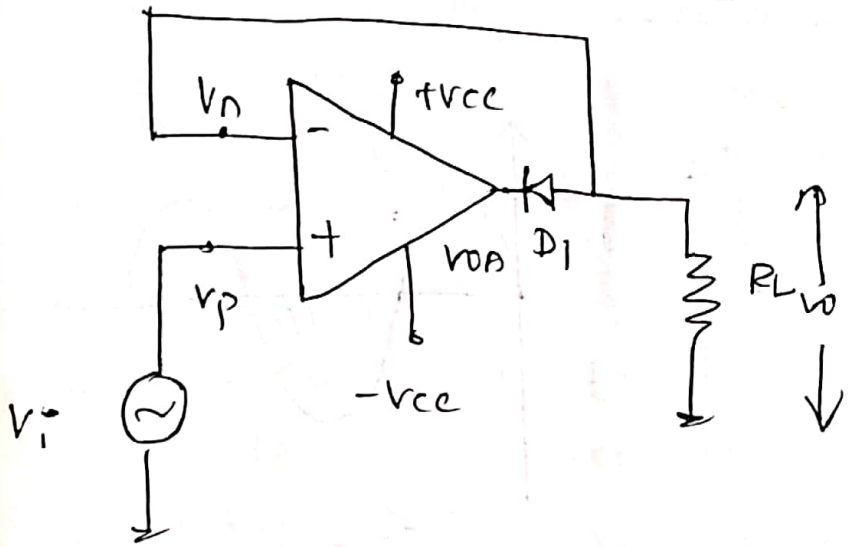


Fig 2.17.4 negative precision half wave rectifier.

this reverse biases the diode making it open. Thus $V_o = 0$ V as no current can pass through RL.

when $V_i < 0$V (ie) negative going, instantaneously V_{OA} is highly negative which forward biases the diode D_1 making it ON. It acts as short circuit and the circuit acts as a voltage follower.

Hence the output voltage is same as input voltage.

Thus the entire negative half cycle is available across the load. Hence the circuit is called negative half wave rectifier.

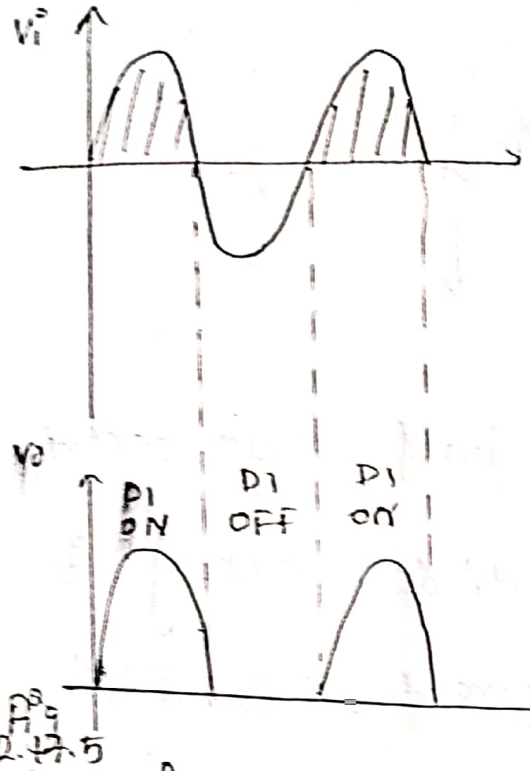


fig 2.17.5 waveforms of half wave rectifier (+ve)

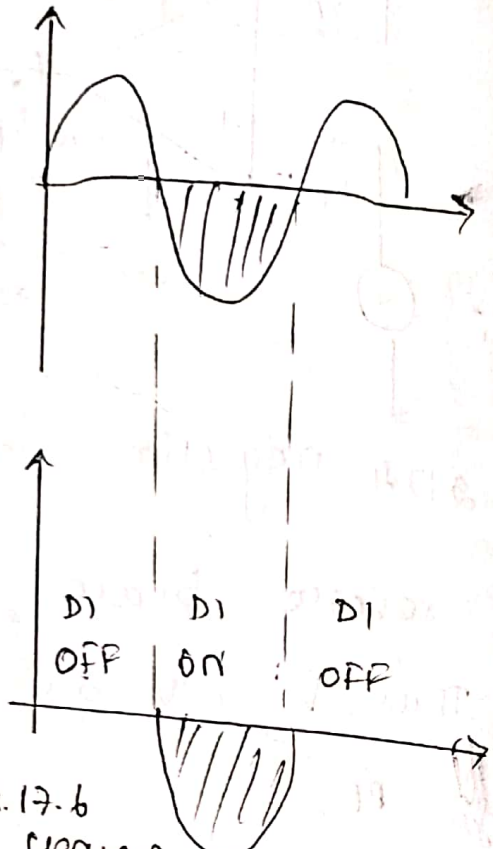


fig 2.17.6 waveforms of half wave rectifier (-ve)

2.17.2 precision full wave rectifiers:-

The full wave rectifier circuits accepts an a.c signal at the input, inverts either negative or the positive half and delivers both the inverted and non inverted halves at the output.

The operation of the positive full wave rectifier is expressed as

$v_o = |v_i|$ for negative rectifier

$v_o = -|v_i|$

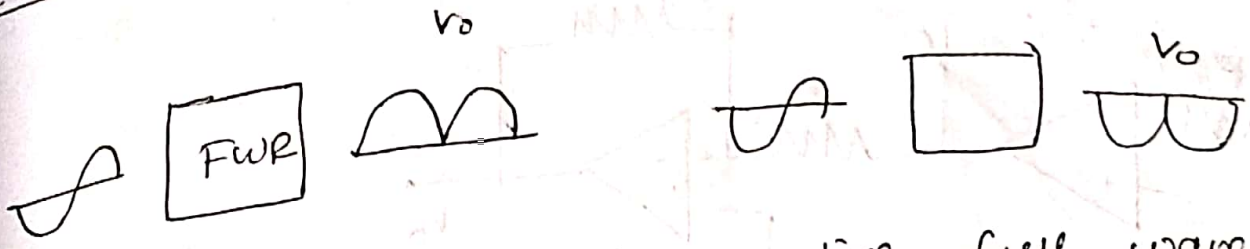


Fig 2.17.8 positive and negative full wave rectifiers.

The precision full wave rectifier circuits are precision absolute value circuits.

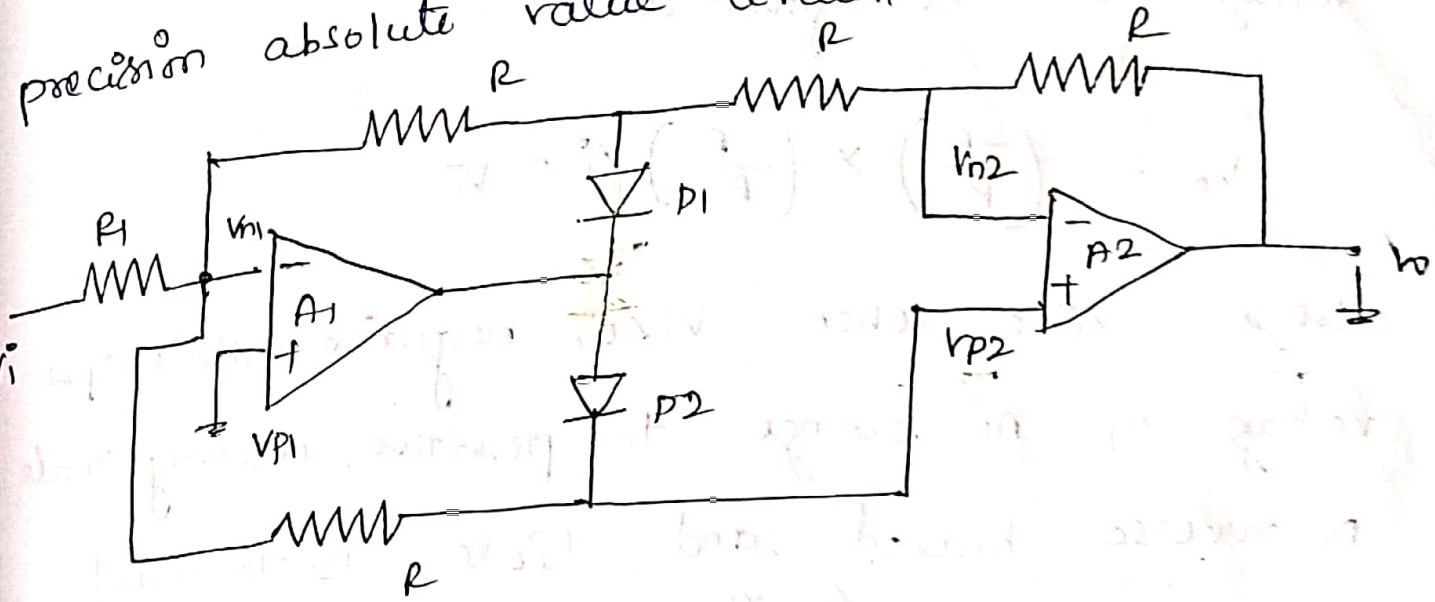
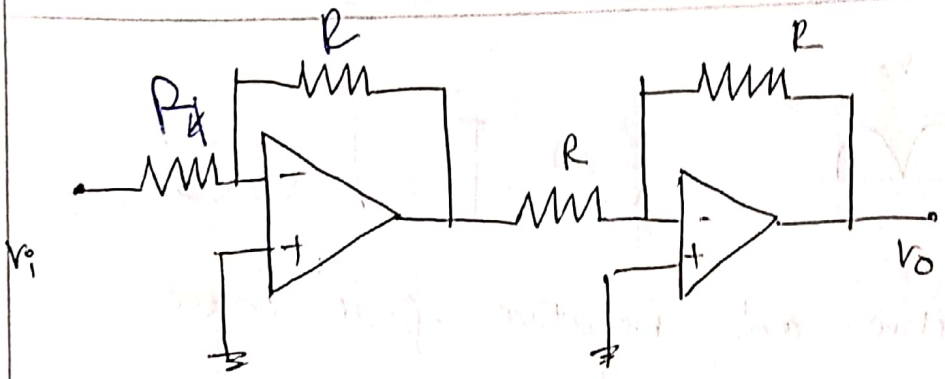


Fig 2.17.9 Full wave rectifier.

case i) : when $V_i > 0$, inverting side of A1 will force its output to swing negative, thus forward biasing D1 and reverse biasing D2.

Since no current flows through resistance R connected between V_{n1} and V_{p2}, both are equipotential. (i.e) $V_{n1} = V_{p2} = 0V$.



From the equivalent circuit the output voltage can be given as

$$V_o = \left(\frac{-R}{R}\right) \times \left(\frac{-R}{R}\right) V_i = V_i$$

case 2 : $v_i < 0$ when $V_i < 0$, negative the output voltage of A_1 swings to positive, making Diode D_1 reverse biased and diode D_2 forward biased.

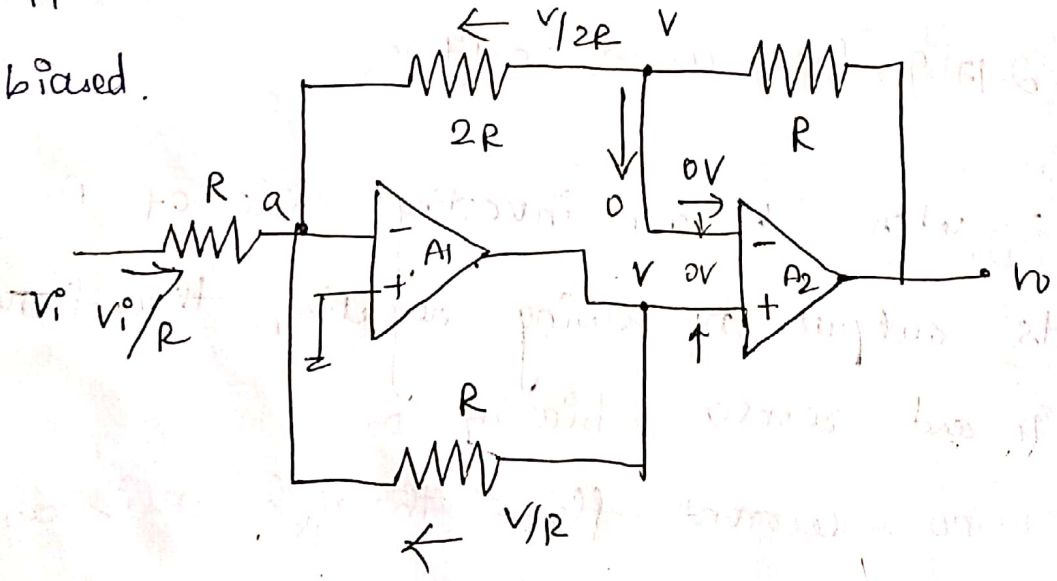


Fig 2.17.b Equivalent circuit

Let the output voltage of opamp A_1 be V.

Since the differential input to A_2 is zero.

the investing input terminal is also at voltage V.

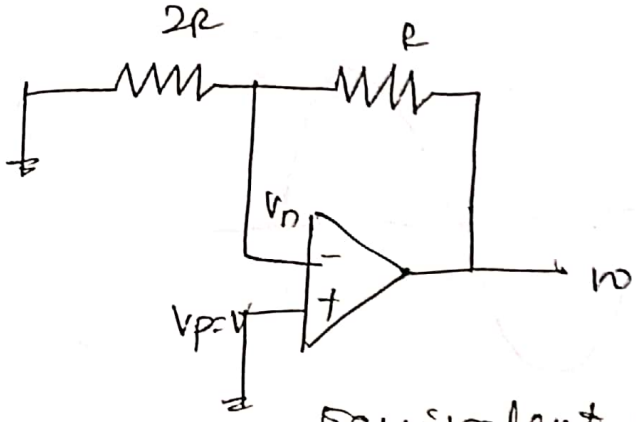


Fig 2.17.11 Equivalent circuit.

Applying KCL at node a we have

$$\frac{V_i}{R} + \frac{V}{2R} + \frac{V}{R} = 0$$

$$\frac{3V}{2R} = -\frac{V_i}{R}$$

$$V = -\frac{2}{3} V_i$$

To find v_o interms of V we Concentrate on the equivalent circuit of A2

$$V_o = \left(1 + \frac{R}{2R}\right)V = \left(\frac{2R+R}{2R}\right)V = \frac{3R}{2R} V = \frac{3}{2} V$$

$$\therefore \quad V_o = \frac{3}{2} \times \frac{-2}{3} \times V_i$$

$$\boxed{V_o = -V_i}$$

Hence for $V_i < 0$ the output is positive.

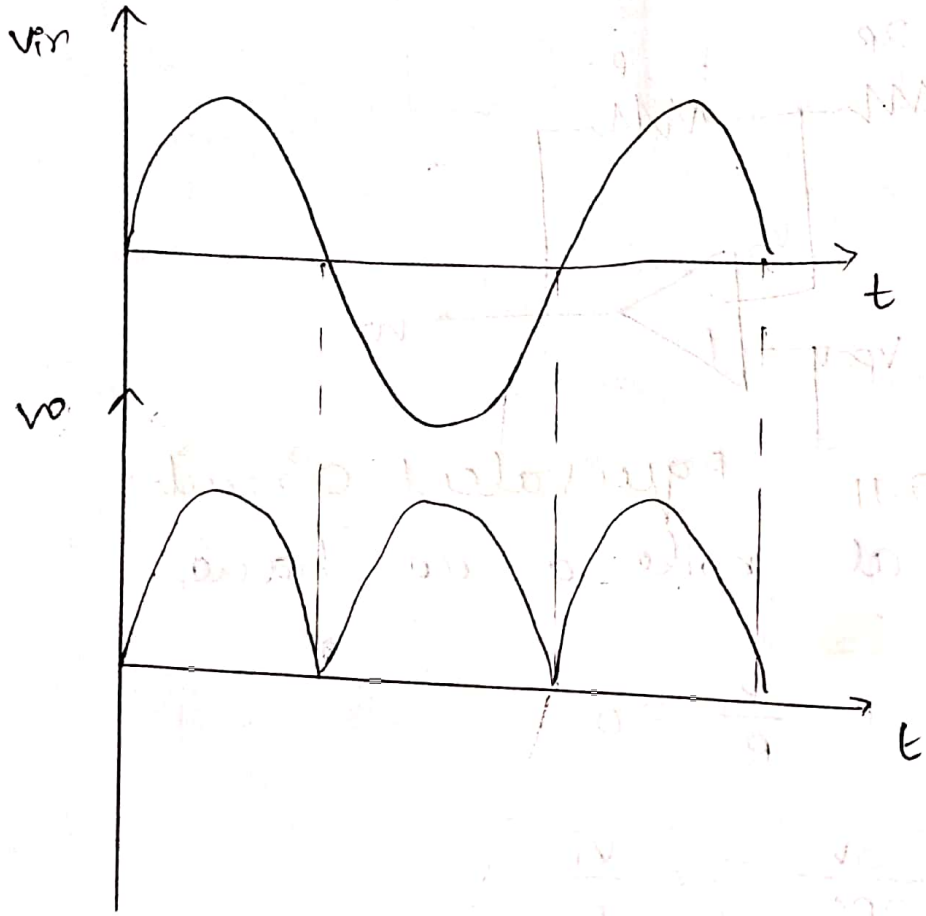


Fig 2.19.12 Input and output waveforms for full wave rectifier.

2.20 Active filters :

A filter is a circuit that is designed to pass a specified band of frequencies while attenuating all the signals outside that band. It is a frequency selective circuit.

The filters are basically classified as Active filters and passive filter.

The passive filter networks use only passive elements such as resistors, inductors and capacitors.

On the other hand, active filter circuits use the active elements such as op-amps, transistors alongwith the resistors, Inductors and capacitors.

2.20.1 Advantages of Active filters :

1) All the elements alongwith Op-amp can be used in the integrated form. Hence there is reduction is size and weight.

2) The cost of the integrated circuit can be much lower than its equivalent passive network.

3) Due to availability of modern ICs, variety of cheaper opamps are available.

4) The inductors are absent in active filters hence the modern active filters are more economical.

5) The design procedure is simpler than that for the passive filters.

Inspite of the above advantages, the active filters also have certain limitations,

1) The finite bandwidth of the active devices place a limit on the highest frequency of operation.

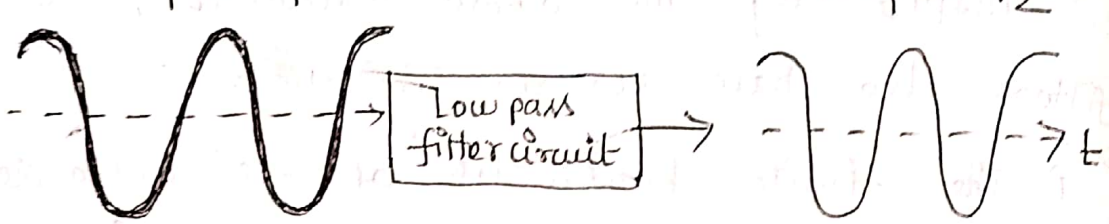
2) Another important factor is the sensitivity. The active elements are much more sensitive to the temperature and the environmental changes than the passive elements.

3) The requirement of d.c power supply is another disadvantage of the active filters. The most commonly used filters are

1) Low pass filter (LP)
2) High pass filter (HP)
3) Band pass filter (BP)
4) Band Reject filter (BR)
5) All pass filter.

2.20.2 Concept of filter and frequency response

The first basic type of filter is low pass filter. As the name suggests, it passes low frequency signal from input to output while it blocks high frequency signals from input.



Signal with hassh

output removing hash from input.

Fig 2.20.1 Concept of low pass filtering

The input voltage V_1 has a low frequency signal alongwith some unwanted high frequency signals. The unwanted high frequency signals are called hash and are generated due to noise.

The function of low pass filter is to remove this hash from input and to produce low frequency signal output.

Thus the low pass filter is a circuit which passes the low frequency signals from

input to output, rejecting the high frequency signals.

Frequency response:

The frequency response of the filters are shown in figure. where dashed curve indicates the ideal response and solid curve shows the practical filter response.

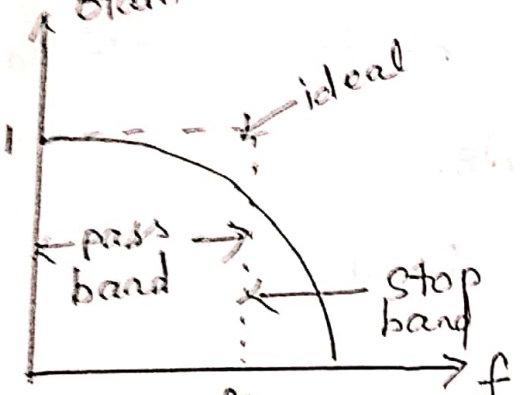
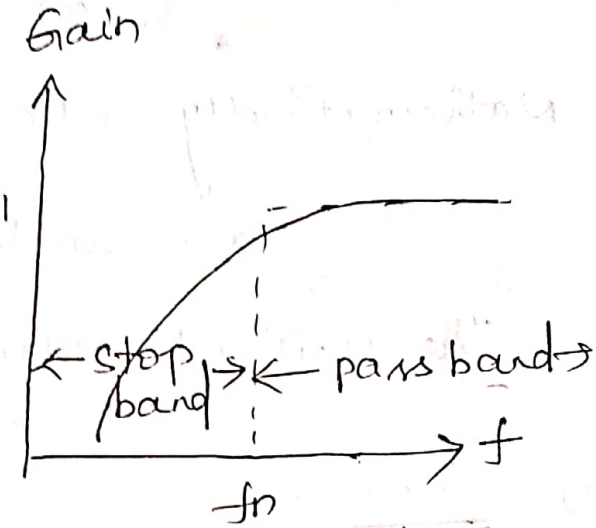
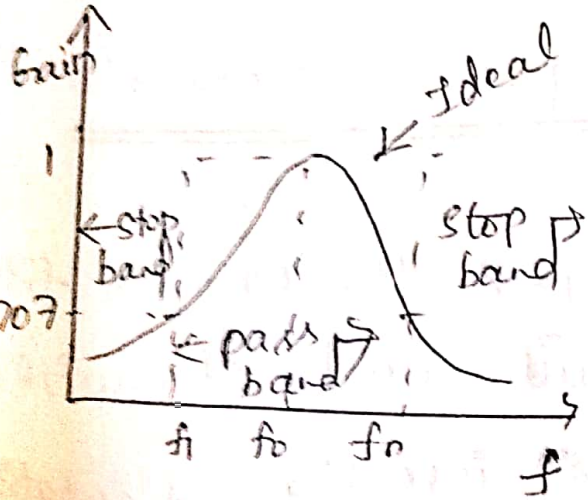


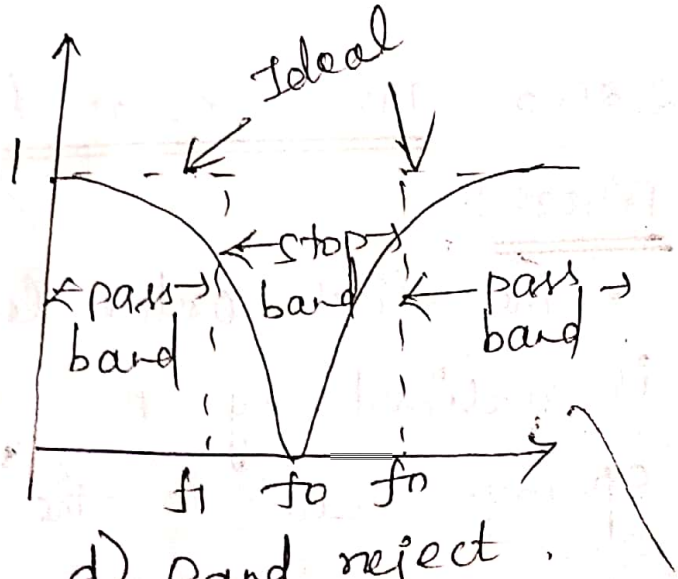
Fig 2.20.2 Low pass fn a) Frequency response of filters



b) High pass



c) Band pass



d) Band reject.

1) Transfer function :-

It is defined as the ratio of Laplace transform of output to Laplace transform of input. It is denoted as : H(s). Replacing the variable s by jω we get the frequency domain transfer function H(jω).

$$H(s) = \frac{V_o(s)}{V_{in}(s)} \qquad H(j\omega) = \frac{V_o(j\omega)}{V_{in}(j\omega)}$$

Mathematically attenuation or loss is defined as

$$\alpha = -20 \log |H| \text{ dB}.$$

The unit of attenuation in dB.

2) Gain :-

Gain is defined as

$$A = 20 \log |H| \text{ dB}.$$

2.20.3 First order low pass Butterworth filters :-

The first order low pass Butterworth filter is realised by R-C circuit used alongwith an Op-amp used in the non inverting configuration.

The resistances R_f and R_1 decide the gain of the filter in the pass band.

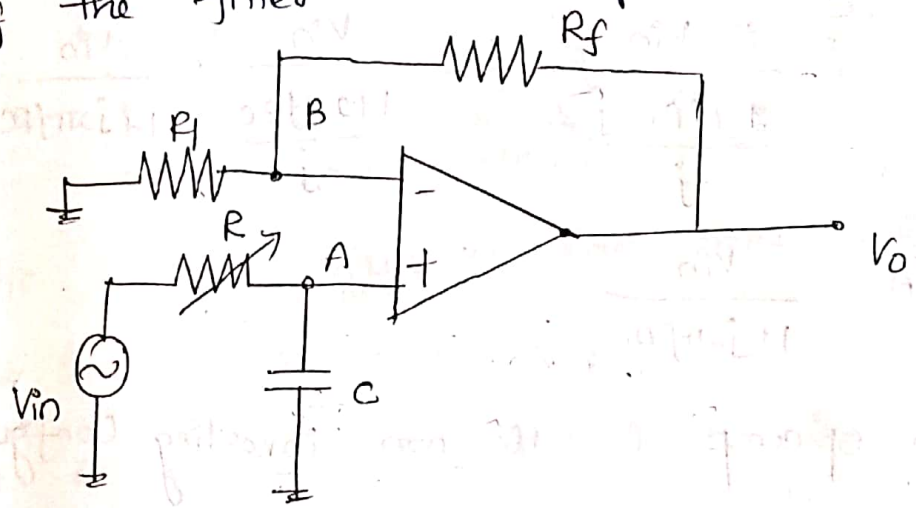


Fig 2.20.3 First order low pass Butterworth filter.

2.20.3.1 Analysis of the filter circuit.

The impedance of the capacitor c is $-jX_C$ where X_C is the capacitive reactance given by

$$X_C = \frac{1}{2\pi fc}.$$

By the potential divider rule, the voltage at the non inverting input terminal A is given by

$$V_A = \frac{-jX_C}{R-jX_C} V_{in}$$

$$= \frac{-j\frac{1}{2\pi fc}}{R-j\frac{1}{2\pi fc}} V_{in} = \frac{\frac{-j}{2\pi fc}}{\frac{2\pi fRc-j}{2\pi fc}} V_{in}$$

$$= \frac{-j}{2\pi fRC - j} V_{in}$$

$$= \frac{V_{in}}{\frac{2\pi fRC - j}{-j}} = \frac{V_{in}}{\frac{1 + 2\pi fRC}{-j}} = \frac{V_{in}}{1 + j2\pi fRC}$$

$$V_A = \frac{V_{in}}{1 + j2\pi fRC}.$$

As the opamp is the non inresting configuration

$$V_o = \left(1 + \frac{R_f}{R_1}\right) V_A$$

$$V_o = \left(1 + \frac{R_f}{R_1}\right) \frac{V_{in}}{(1 + j2\pi fRC)}$$

$$\frac{V_o}{V_{in}} = \frac{AF}{1 + j\left(\frac{f}{f_H}\right)}$$

$A_F = \left(1 + \frac{R_f}{R_1}\right)$ = Gain of filter in pass band.

$f_H = \frac{1}{2\pi RC}$ = high cut off frequency of filter.

f → operating frequency.

The $\frac{V_o}{V_{in}}$ is the transfer function of filter and can be expressed in the polar form.

$$\frac{V_o}{V_{in}} = \left|\frac{V_o}{V_{in}}\right| \angle \phi$$

$$\left|\frac{V_o}{V_{in}}\right| = \frac{AF}{\sqrt{1+(f/f_H)^2}} \quad \text{and} \quad \phi = \tan^{-1}\left(\frac{f}{f_H}\right).$$

the above equation describes the behaviour of the low pass filter

1) At very low frequencies $f < f_H$, $\left|\frac{V_o}{V_{in}}\right| = AF$ (i.e) constant.

2) At $f = f_H$, $\left|\frac{V_o}{V_{in}}\right| = \frac{AF}{\sqrt{2}} = 0.707\,AF$ (i.e) 3 dB down to the level of AF.

3) At $f > f_H$, $\left|\frac{V_o}{V_{in}}\right| < AF$

Thus for the range of frequencies, $0 < f < f_H$ the gain is almost constant equal to f_H which is high cut off frequency

At $f = f_H$ gain reduces to 0.707 AF.

As the frequency increases, the gain decreases at a rate of 20 dB/decade.

The frequency f_H is called cut off frequency, break frequency, -3dB frequency or corner frequency.

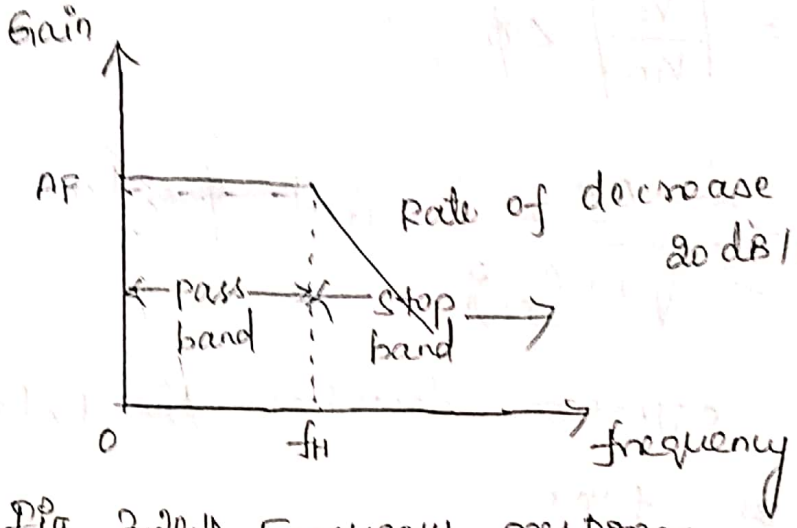


Fig 2.20.4 Frequency response

2.20.3.2 Design Steps:

The design steps for the first order low pass Butterworth filter are

1) Choose the cut off frequency f_H.

2) Choose the capacitance C usually between 0.001 and 1MF. Generally it selected as 1 MF or less than that.

3) For the RC circuit

$$f_H = \frac{1}{2\pi RC}$$

Hence as f_H and C are known, calculate the value of R.

4) The resistances R_f and R_1 can be selected depending on the required gain in the pass band. $A_F = 1 + \frac{R_f}{R_1}$

Once the filter is designed, it is necessary to change the value of cut off frequency f_H. The methods used to change the original cut off frequency f_H to a new cut off frequency f_{H1} is called as frequency scaling.

Problem : Design a low pass filter using op-amp at a cut off frequency of 1 KHz with pass gain of 2.

Solution : Given : $f_H = 1KHZ$

$A = 2$.

Step 1 : cut off frequency $f_H = 1KHZ$.

Step 2 : Choose $C = 0.01\ \mu F$.

Step 3 : $f_H = \frac{1}{2\pi RC}$ (or) $1 \times 10^3 = \frac{1}{2\pi R \times 0.01 \times 10^{-6}}$

$$\Rightarrow R = \frac{1}{2\pi \times 1 \times 10^3 \times 0.01 \times 10^{-6}}$$

$$\boxed{R = 15.91 K\Omega}$$

Step 4 : $A_F = 1 + \frac{R_f}{R_1}$

$2 = 1 + R_f/R_1 \Rightarrow R_f/R_1 = 1$

$R_f = R_1$

$\therefore \quad R_f = R_1 = 10\,k\Omega$